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ELECTRONICS &
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# CONTENTS

January 1986
Volume 92
Number 1599

## FEATURES



## REGULARS




**Produced on an Omnicomp graphics display controller, this month's cover is an example of what can be produced using modern, high-speed digital electronics and data-conversion devices.**

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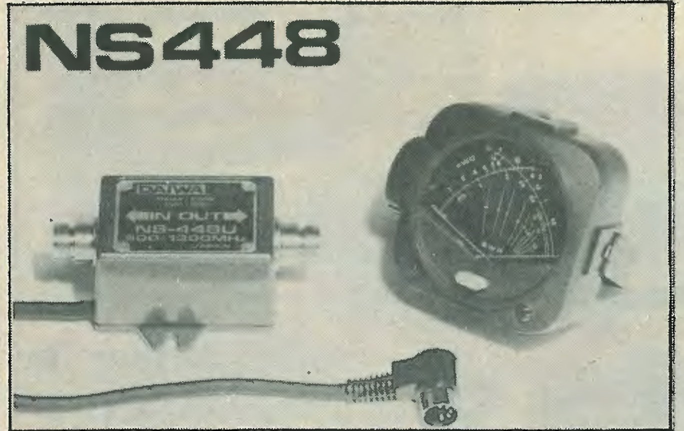

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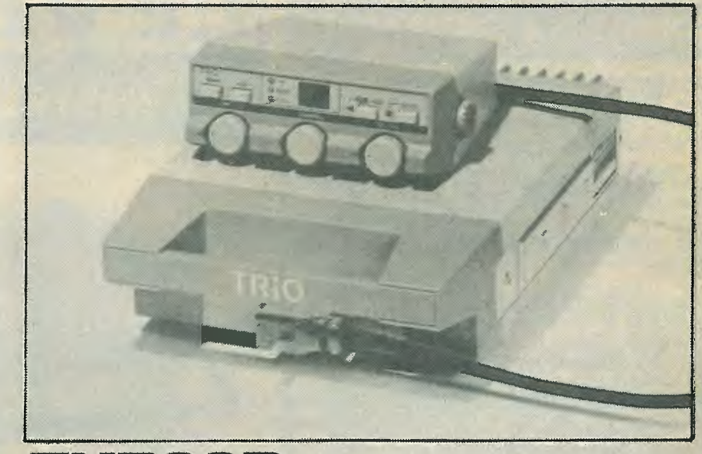


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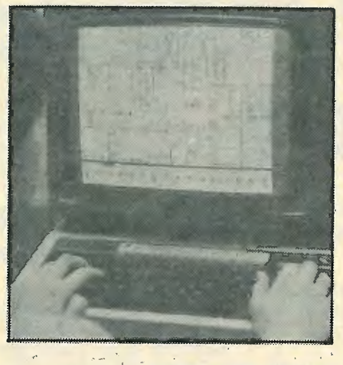

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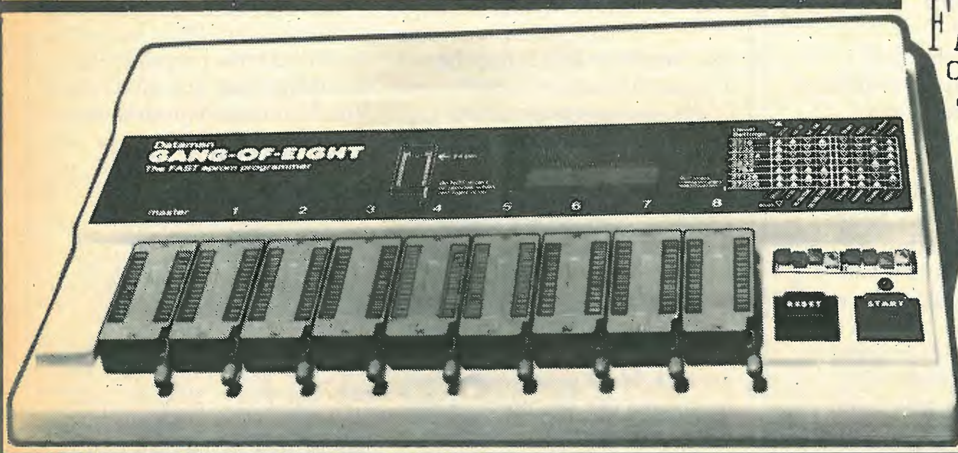


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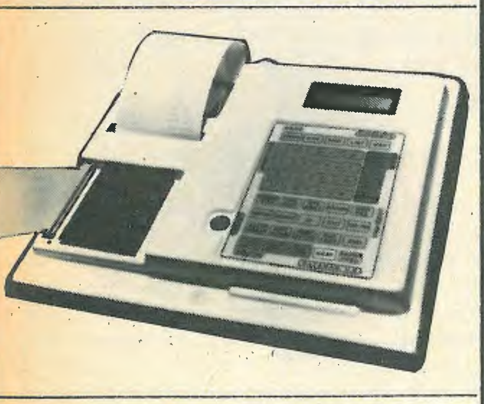

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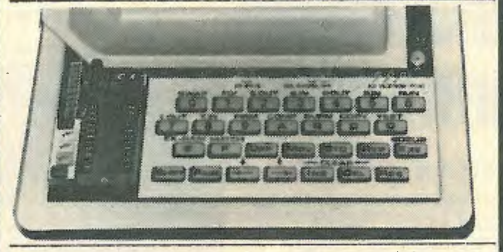

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# Von Neumann's elephants

It is fifty years since the publication of Alan Turing's seminal paper, *On computable numbers,* which is generally considered to signal the birth of modern computers. It embodies the system known as Von Neumann's computer architecture, which incorporates sequential programs and can still be recognized in the latest computer devices.

All the major integrated circuit manufacturers have now announced their 32-bit processors. These can access millions of bytes of memory and their operation is measured in 'mips' — millions of instructions per second. As each of the instructions can offer the functions of three or four of the instructions on their predecessors, this makes them even faster. Because they are so fast, they can do several tasks apparently simultaneously by switching rapidly between them.

All this seems very impressive. But why is there a niggling feeling that they are not as good as they seem? Perhaps it's because they are, in the final analysis, just inflated versions of the earliest processors.

At the same time some (mostly much smaller) manufacturers have been looking at new concepts and several have now come up with reduced-instruction-set computer (r.i.s.c.) processors, which tackle the problem in a very different way. They divide the data up into little packets and attach labels to them: the labels direct them through the chosen processes and reassemble the processed data. No longer do they have to queue up to go through the mill, however fast it may be; and, as the tasks assign the labels, the computer can do several different things concurrently. Consequently, processes are very fast and efficient. Another difference is that they are designed to run a specific low-level language and do not have to include all the instructions that may be necessary to be universal devices. Most of the high-level languages can be compiled and run on these devices and it is possible to use them exactly as if they were the universal devices of the other manufacturers. They also use very-large-scale integration with a similar complexity in circuitry and occupy much the same area of silicon.

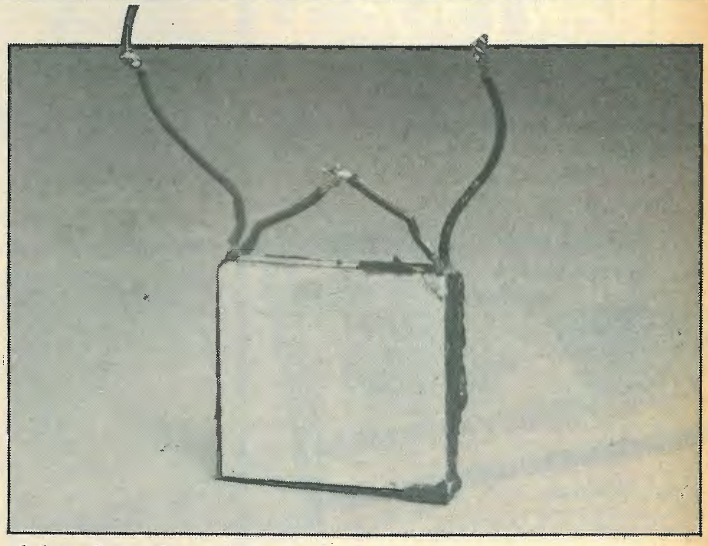
So why should anyone bother with the new r.i.s.c. processors? The reason lies in the future. Many computer scientists have complained about the built-in limitations of Von Neumann's 'architecture.'

It may be possible to make conventional processors even larger (64-bit devices are already under development) and even faster by reducing the physical size on the silicon chip and/or by using gallium arsenide but the basis on which they are built is now fifty years old. The r.i.s.c. devices point forward to a new technology, a lateral step in the evolution of computer science.

If the early microprocessors can be likened to mice, then the new generation have grown into elephants. The escape from the limitations of Von Neumann's system heralds the 'fifth-generation' computer much more than advances in very-large-scale-integration in silicon or gallium arsenide.

# Thermal semiconductors

A solid-state heat pump is being developed and manufactured in the UK by a US Army general. When Werner von Braun's rockets became too hot he called on a major in the US Army to help provide cooling equipment. The major, now General Laurance Davis, devised an electronic device for cooling the rockets. Since his retirement from the army, he is marketing commercially the device for which he is the patentee. The device is a wafer made up from tiny cubes of crystalline metallic bismuth, doped to provide a semiconductor action. 245 of the cubes are joined in series, alternately P and N-type material, to produce 488 p-n junction diodes. The chain of diodes is sandwiched between two thin layers of a ceramic material to produce a wafer, 50 by 50mm, about 2mm thick. When a direct current is applied across the wafer, one side gets hot and the other cold. This is a similar action to that found in the Peltier bimetallic junction described in 1840, but that exercise was only of academic interest with a slight temperature difference. With a potential difference across the wafer of 6.5V, the cold side falls rapidly to −40°C while the hot side rises to 57.2°C. Wafers can be cascaded to produce even grater temperature differences. When the current is reversed, the sides reverse their functions, the hot side becoming cold and *vice versa.*



**A hand-made prototype heat-pump semiconductor wafer. consisting of 245 tiny cubes of doped bismuth, it can develop a temperature difference of 97.2°C between its ceramic checks.**

Applications are numerous but a few interesting ones have been postulated:

A room heater could be about the size of a telephone, containing nine of the wafers. It should be able to heat an average room area and use 40% less power than conventional methods: An instant ice-cube tray will freeze water in less than a minute: other domestic uses include refrigerators, freezers, plate warmers, slow cookers and some of the functions can be combined by using both sides of the wafers: for car heating or cooling the device uses practically no engine power while the conventional car air-conditioner can consume up to 5bhp. The wafers can also be used for the refrigeration of food in transit, cooling electronic equipment, and in medicine for freezing tissue.

The wafers are still at the development stage. Factories are to be set up in London and the company expects to employ 1000 people.



# IEE and IERE to merge

Members of the Institute of Electrical Engineers and the Institution of Electronic and Radio Engineers are invited to take part in a debate on the proposed merger between the two. The councils of both institutions have welcomed the proposal but the final decision will be taken after special general meetings for each body to be held towards the end of 1986. If approved there would be a transitional period before the final merger which should take place towards the end of 1988.

The merger was the primary recommendation of a special working party composed of senior officers of both institutions. Their report stated that if the two institutions should come together, the new body would speak with greater authority to government, the Engineering Council and other organizations and the public. The combined institution would also have more authority in the international sphere. It would offer better services and publications to its members; a strengthening and broadening of interests in electronics, communications, and information engineering; a common standard for chartered engineers' status; and a single body to accredit training courses and programmes. The working party was set up at the beginning of 1984 to explore the possibility and recommend terms for a merger between the institutions. The IEE has about 83 000 members and the IERE just over 13 000. 1111 members belong to both bodies.

The joint body will be known as the Institution of Electrical Engineers. The Institution was the first of its type in the world. The 1921 charter would be maintained with its precedence over more recent charters. However, the IEE will broaden its terms of reference to bring in the electronics and communications areas of the specialist members of the IERE.

**Monitoring equipment at the Department of Trade's station near Baldock in Hertfordshire, which can cover the spectrum from 10kHz to over 12GHz.**

# Radio spectrum guide

For the first time, the Government has made available a list of UK radio frequency allocations. In a 310-page paperback book, the Department of Trade catalogues the bands from 9kHz to 400GHz with their uses both in Britain and abroad.

For each band or sub-band, a table shows the UK assignments alongside a table of the corresponding ITU allocations. The guide describes in detail the band plans for some of the most widely-used radio services — though only for bands occupied by non-government users.

The new publication is one of the fruits of the Merriman committee's pressure for greater openness in radio administration. However, the ministerial instinct for secrecy has ensured that large tracts of spectrum are labelled with nothing more specific than 'Government'.

Five annexes provide further information on bands available to certain services, including private mobile radio, private fixed links, low-power systems, radio astronomy and amateur radio.

No regular updates of the guide are planned, though the Department intends to revise it in the event of any major reorganization of the spectrum. Minor alterations (such as the recent introduction of a 50MHz amateur allocation, which, incidentally, came too late for the present edition) will be covered by amendment sheets.

The guide, United Kingdom Table of Radio Frequency Allocations, is published by Her Majesty's Stationery Office at £12.

# Structured systems aid efficiency

A greater understanding of the requirement of computerized tools for the support and development of data processing systems is provided by SSADM, structured systems analysis and design method. Developed for the Central Computer and Telecommunication Agency, SSADM has been used on nearly 200 projects in government departments and is finding a wider market in the private sector. It provides a coherent, integrated set of standards, procedures, techniques and tools with the aim of achieving a significant reduction in systems development and maintenance costs.

The Agency is to collaborate with the National Computer Centre in the promotion, development and support of SSADM by providing jointly Training materials and courses, books and reference manuals, and implementation support for new users. The collaboration should ensure the long-term availability and support for this method of operation and could lead to an integrated project support environment for the system.

# BT challenges

The de-nationalization of British Telecom also removed its monopoly on telecommunications and we have news of three services which are planning to compete with BT. Timefame International, who are a major information provider on Prestel, are to set up their own public viewdata service. Their database will, they claim, overcome Prestel's shortcomings by eliminating delays in logging-on, and easing the routing to specific pages of information. There will be no page charges and information providers will be able to edit their own pages directly. The capacity of the system will be 17 million pages (Prestel has 1.5 million) and the prices will be "significantly cheaper" than those for Prestel. Telelink magazine who reported the story says that Timefame will not officially confirm the launch of the database but that they have received undisclosed US backing to investigate such a service and that they have the capability to put it into action.

Telemessages, you will remember, have replaced telegrams in the UK. The message is delivered with the post rather than the old system of sending a boy round as soon as it is received. Microlink are planning to offer a telemessage service with which any micro/modem user can send a message direct form the home/office keyboard which will be delivered by the post the morning after transmission. What is especially significant is that they plan to do it at a fraction of the BT cost.

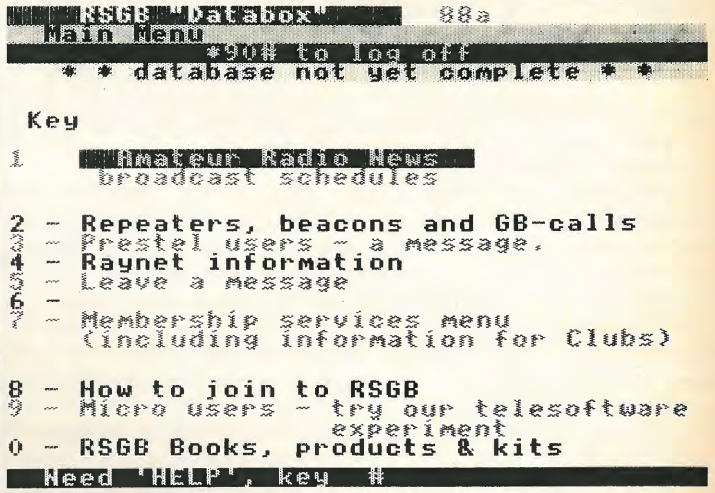
Comprehensive Communications is a company set up to market BATB approved telephone equipment under its own brandname. Their particular target is the home and small business market through a network of local authorized distributors and high-street shops. They have recruited two top salesmen, Clive Davison and Dennis Woolford, who were formerly senior managers at BT Consumer Products.

# Engineers better off

A survey by the Engineering Council has reported that more than 59% of chartered engineers now earn more than £15k, compared with 32% two years ago. The majority of them would happily recommend a career in engineering to young people. The 1985 survey of chartered and technician engineers questioned 28 thousand engineers, selected at random from the Council's register. Dr Kenneth Miller, director-general of the Council, said: "It is pleasing to note that earning have increased at a rate higher than inflation, and also that the level of unemployment is gratifyingly low among chartered and technician engineers — less than 1% at any time during the year."

73% of the chartered engineers were graduates and their salaries tend to increase throughout their careers, while non-graduate engineers often show no real increase in earnings after their early forties. The highest earning were found in nationalized industries while the lowest were paid to engineers employed in local authorities. However just under half of the engineers surveyed were members of trades unions and over a quarter of these belonged to NALGO.

Supervisory staff and management administrators received the highest incomes; next were those in commercial or consultancy areas. The top paying industries, ranked in order were petroleum and petrochemicals, electricity generation, postal services, telecommunications and broadcasting.

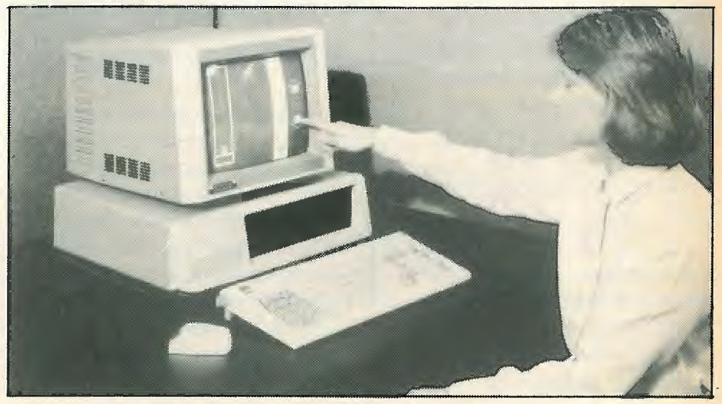



**A quick answer to many of the questions most often asked about amateur radio is provided by the Radio Society of Great Britain's new Databox service. The system contains up-to-date news of the amateur world and of the RSGB's activities and it even includes some telesoftware: if you have a Prestel-type terminal, call it on Potters Bar (0707) 52242.**

# Don't send the bill, just the data

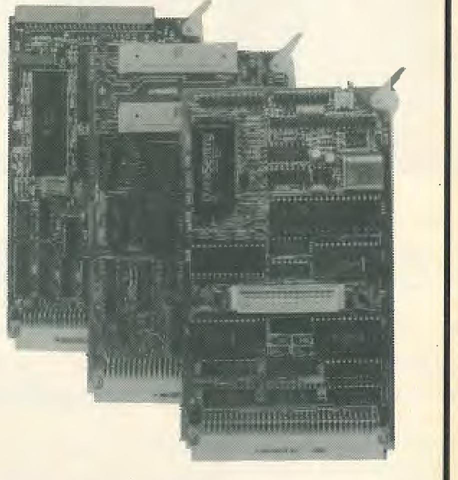
A joint venture between McDonnel Douglas Information Systems and BT is aimed at cutting the cost of business transactions. The new company, called Edinet, will provide electronic data interchange to give direct computer-to-computer exchange of business documents such as purchase orders, invoices and statements. Documents are coded in such a way as to reconcile differences between computers and the physical layout of the document. The system has been successful in the USA where more than 200 companies are already connected to the network. The UK company will initially rely on US processing resources and be connected through BT's PSS data network. Potential customers will be encouraged to conform to the international open standards for document interchange as the Edinet service itself conforms.

**A computer system designed specifically for training has been developed by Marconi Instruments. Mandarin incorporated a touch-sensitive screen and a mouse and moves from step to step according to the user's response.**



# RM65 . . . The professional choice

The RM65 range of Eurocard modules has been designed to meet the needs of engineers implementing microcomputer systems for control and industrial applications.



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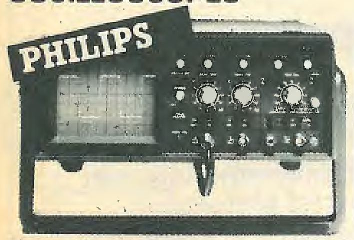


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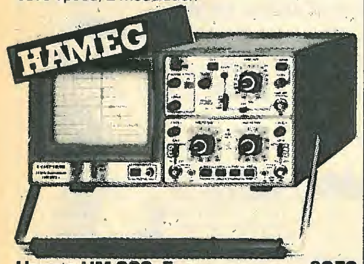


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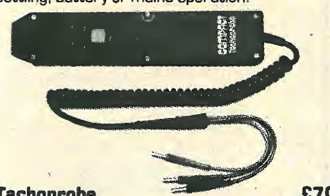

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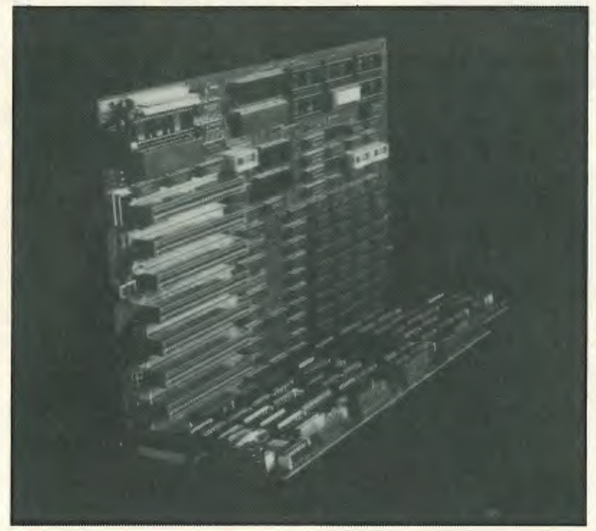

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# Remotely tunable antennas for frequency-hopping

by Charles E. Cooper

## PIN-diode selection of inductors allows antenna tuning at rates up to about 1000 per second

One of the means by which military communications are rendered secure against enemy eavesdropping is the process of frequency-agility or "hopping", whereby the carrier frequency is repetitively changed at rates of up to a thousand per second, according to some pre-arranged random pattern, between (for example) any of the 7000 channels spaced 25kHz within 225-400MHz.

The pattern of frequency changes or "hops" can be varied whenever necessary to maintain security and must, of course, be known to and followed by both (or all) terminals of the intended communications chain. The system of hopping can be applicable whether the carrier conveys information by amplitude or frequency modulation, or as logic data.

All elements of the communication system must be able to produce or follow the frequency-agile carrier, including all antennas used for any combination of ground and air paths. Self-evidently, the antenna requirement for frequency-agile capability is most conveniently met by fully broadbanded designs, covering the full frequency range without tuning or other adjustment, in circumstances where acceptable dimensions make this possible.

Figure 1 shows the relative dimensions and form of a representative selection of antenna blade designs for airborne service. All of them are substantially two-dimensional, with cross-sections approximating to various aerodynamic standards. Outlines A and B are typical of various manufacturers' versions of well-proven solid-blade antennas which have been loss-free broadbanded across the u.h.f. band 225/400MHz, within a v.s.w.r. limit usually 2.0:1. They commonly achieve power-efficiency better than 90% which, with the radiation pattern typical of quarter-wave unipoles, is equivalent to about + 2dBI (or 2 dB above the response of a theoretical loss-free isotropic raidator).

The basic v.h.f. band, 116-156MHz is similarly well covered but, as shown in the outline of Fig. 1(B), within housing shell heights of 35 to 40 cm, which has become more or less unacceptable for fast, highly manoeuvrable aircraft. Even within this height, extension to coverage of the full v.h.f. and maritime bands, 100-174MHz, requires that broadbanding techniques be supplemented by some degree of resistive damping, to maintain an acceptable limit of v.s.w.r. The same shell example has also been used to house separate radiating elements for the 100-174 and 225-400MHz bands, usually diplexed for onward connection via a common terminal.

More recently, the same shell example has been used to function across the Tactical v.h.f. band, 30-88MHz. However, at the low-frequency extreme of this band, the height represents less than λ/25, and the resultant very low equivalent radiation resistance renders broadbanding ineffective. These designs therefore comprise a simple plate radiator to cover all three bands, fed via a frequency-dependent attenua-

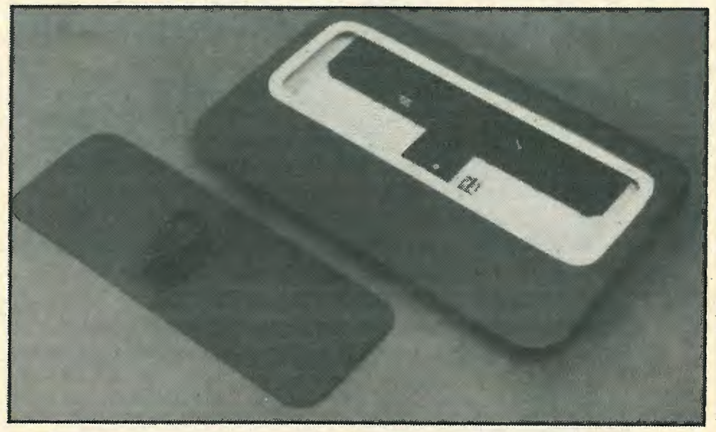


Fig. 2. Housing of antenna in vertical fin of PAH1 helicopter.

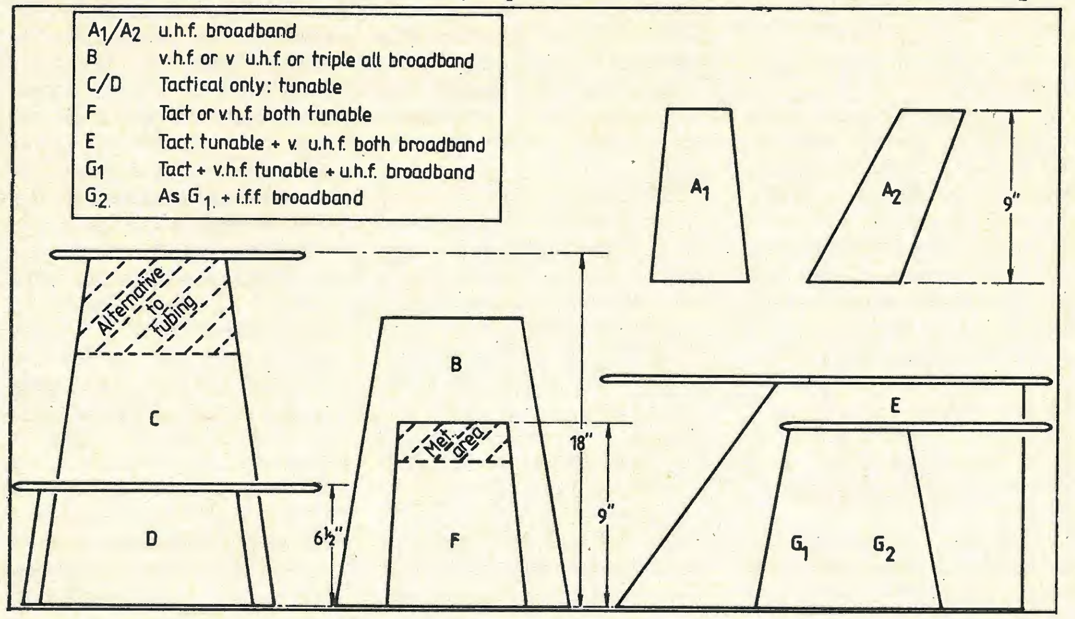



Fig. 1. Selection of blade antenna shapes.

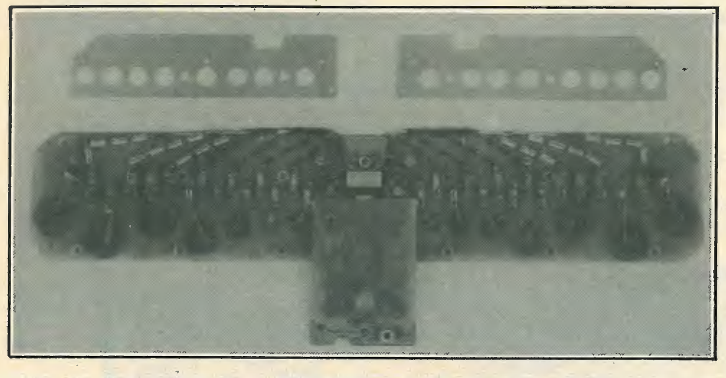


Fig. 3. Tunable dipole assembly to fit inside fin.

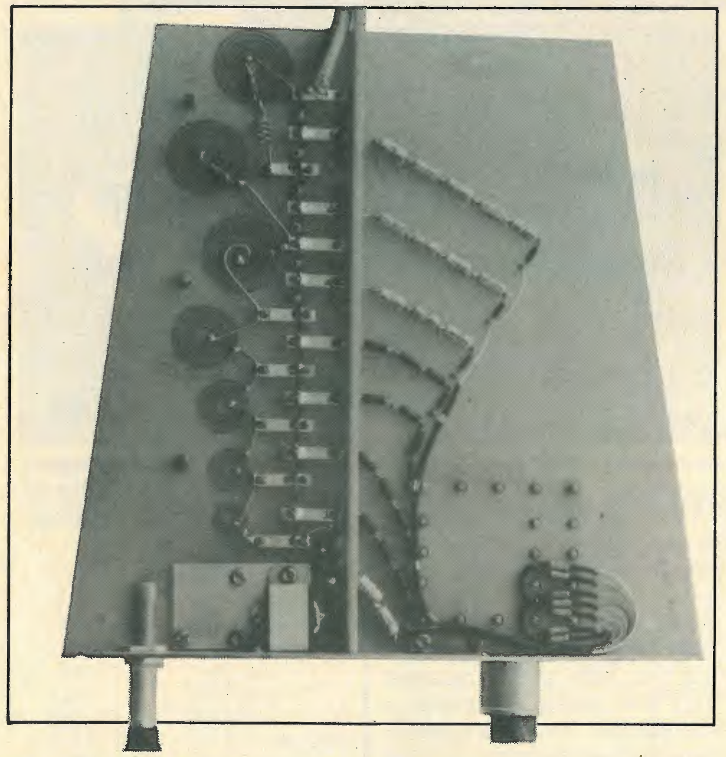


Fig.4. Printed-circuit tuning assembly.

tor which inserts sufficient resistive loss to maintain v.s.w.r. below about 2.5:1 At 30MHz, the inserted loss reduces radiation capability to about −25 dBI.

It is perhaps a tribute to the sensitivity of current receivers that such abysmal antenna performance has been even moderately acceptable, but inevitable deficiency of communication range has produced demands for considerable improvement. Prior to the advent of frequency-agility, the requirement was met by antenna designs tuned via miniature high-vacuum, high-voltage relays but these were quite unable to cope with "hopping" systems.

Extensive new building of the MBB B0105 helicopter in its PAH1 military version provided the stimulus for first development of Tactical-v.h.f. antennas tunable for high efficiency, and controlled via PIN diodes for fast retuning. At this time, with only helicopter usage envisaged, the dimensional restrictions were not too severe.

Two variants were first produced: a unipole design housed within a glass fibre shell 46 cm high, as in Fig. 1(C) for fitting externally, and a dipole design in skeleton form to be housed within one of the two vertical stabilizer fins of the PAH1 helicopter. The close-up of the port fin, Fig. 2, shows the tunable dipole detailed in Fig. 3. It is basically a handed-pair of the printed-circuit tuning assembly shown in Fig. 4, used singly in the unipole version, and which is mounted on the cabin roof.

The dipole radiates via metallized areas at top and bottom of the fin, while the unipole version radiates via a short length of metal tubing fixed to the top of the housing shell. A later version substituted an internal plate as the radiator. Altogether, about 800 of these two antennas have been in service on German and Spanish military helicopters, for periods up to three years.

Expressly for fitting underneath an aircraft type having very little ground clearance, the unipole variant shown in Fig. 5 was produced for housing within the 22 cm shell outlined in Fig. 1(D) again covering only the 30-88MHz band. Several skeleton versions of the unipole were produced for suppression within, for example, the fincaps of B.Ae. "Hawk" and Macchi MB329 aircraft.

The basic 30-88MHz tuning assembly was also fitted into externally-mounting shells large enough to house broadbanded v.h.f. and u.h.f. radiators, either separately fed, or diplexed to a common terminal. The example shown in Fig. 6, to the outline of Fig. 1(E) uses the forward tubing section as 30-88MHz radiator, with the shorter, aft section assisting radiation within the 100-174MHz band. This shell was designed with sufficient strength for service on very high-performance aircraft, but its aerodynamic effects have been considered undesirable except on helicopters or the larger fixed-wing aircraft.

Logistics favours commonality between equipment items fitted to the widest range of aircraft types, requiring that the larger market for helicopter antennas be met within parameters suitable for even the most manoeuvrable of fighter aircraft. This total requirement was at first approached by smaller versions of the triple-band resistive-damped antenna previously mentioned, with "gain" performance inevitably still further reduced to around −35 to −40 dBI at 30MHz, which brought forth many complaints about the limited communication ranges achieved.

Accordingly, the 30-88 tunable antenna design form has been re-designed into a shell height around 22 cm, of the outlines shown in Fig. 1(F) and 1(G). Both of these include tunable coverage of the full v.h.f. and maritime bands, 100-107MHz, with the antenna outlined as 1G1 also including broadbanded coverage of the u.h.f. band, both or all bands being diplexed to a common terminal. The version shown as 1G2 further includes the IFF band.

Considering the antenna as a heavily top-loaded monopole, a height of 22 cm results in the radiator impedance being capacitive across the 30-88 and 100-174 bands. With practical capacitance and dimensions of the top-loading conductor, it has a capacitance of some 10-15 pF to the airframe ground plane and, at 30MHz, its series-equivalent radiation resistance $R_r$ will be only a smallish fraction of an ohm. To drive maximum current through $R_r$, the reactance $X_C$ of the radiator capacitance must be balanced or tuned out by equivalent inductive reactance $X_L$, requiring some 2 to 2.5 $\mu$H.

There is no practical and efficient means for varying the radiator capacitance enough to cover the resonant frequency range 30-88MHz and retuning is therefore accomplished principally by changing the value of the series inductance. The means chosen is diode-switched selection from a series-connected group of printed-circuit inductor spirals, having approximately binary-related values and providing setting-steps equal to the value of the smallest inductor. For a required total of, say, 2.4 $\mu$H individual values will be in the series 1.2, 0.6, 0.3, 0.15 etc.

The original antenna of 46 cm height used six inductors, providing 64 possible combinations, and the bandwidth achieved for each setting varied from about 1.3MHz at 30MHz up to at least 6MHz around 80MHz. Tuning was in 1MHz steps, i.e. with each step covering 40 channels at 25 kHz spacing. In consequence of increasing bandwidth towards 88MHz, band-overlap provided considerable redundancy, needing only some 35 steps out of the 64 possible.

Height reduction to 22cm resulted in a lower value of $R_r$, in turn causing bandwidth to fall to about 0.5MHz at 30MHz and hence requiring improved resolution of tuning-setting.



This was done by the addition of a seventh inductor to provide a possible 128 combinations, and by extending tuning into the next decade, that is to steps of 0.1MHz, each now covering only 4 channels at 25MHz spacing. With both the 6 and 7 inductor units, preselection from among excess settings allows for optimization to suit the differing conditions of antenna mounting, particularly of ground-plane area.

With all discrete inductors shorted out-of-circuit, residual strays restricted $F_{o(max)}$ to 88MHz for the 46cm version, but extended above 100MHz for the 22cm, 7-inductor version. For this latter to be extended up to 174MHz, a small capacitor was added into series with the inductor chain, to produce a second group of tuning-settings from combinations of the 3 or 4 smallest inductors. The additional capacitance is shorted out-of-circuit for operation at frequencies below 100MHz.

Much of the achieved performance is determined by manipulation of the unavoidable "stray" impedances and couplings, and is a reason for placing the larger inductor spirals at the elevated end of the series chain, where their capacitance tends best to supplement that of the radiator.

Switching-selection of the reactors utilizes the PIN diode characteristic of maintaining conductivity when signal-current peaks exceed, even grossly, the direct biassing current, provided that the average of current remains well in the conductive direction. The diode charge-storage must maintain conductivity for well above the period of the lowest operating frequency, in this case 30MHz.

Figure 7 shows the conductance characteristic of a suitable diode (though subject to special selection). Desirable increase of conductivity with increase of forward-bias current has to be offset against heat generation within the diode, with restricted opportunity to disperse this heat. Conversely, inadequate conductivity will represent a source of r.f. loss, which, under transmission power, will be an additional heat source. To whatever extent that the diode is imperfectly conductive, its non-linear characteristic generates harmonics, which may well be the ultimate deciding factor in setting the bias level. Values of some 50 to 200 milliamps are used, achieving dynamic conductance values of between 1 and 2.5 mho.

In the reverse-biased non-conductive state, some 10-20 volts is adequate to prevent the diode imposing damping losses under small-signal conditions, and also to maintain diode shunt capacitance at an acceptably low and constant value, as shown in Fig. 8. However, with no current flow, the diode has no charge storage, and will conduct throughout any period when transmission power produces voltage peaks which oppose and exceed the d.c. turn-off bias voltage. Current flow during these periods will be small, due to the high impedances, and will augment the bias voltage through storage in the circuit capacitances. As a result, the apparently inadequate turn-off bias does not generate unacceptable levels of harmonic, although this has had to be reconsidered with increased severity of specification.

For the tuning settings which leave only a single inductor in circuit, this inductor and its shunt switching diode(s) will be subject to the full transmission r.f. voltage, as magnified by the circuit Q which results from the combination of L/C ratio, distribution of strays and by the sum of radiation and all other forms of energy loss. Q is highest for the larger inductors and can cause the r.f. to exceed the ultimate breakdown voltage of the diodes.

This voltage is therefore divided between two or more diodes, centre-tapping certain inductors to ensure equal division of voltage across each diode. A decrease in the effectiveness of shorting-out the inductor has to be accepted, since higher-voltage diodes tend also to be of lower conductivity, unless of larger area, in which case they produce a problem of increased shunt-capacitance. Everything is compromise!

Binary selection can result in both sides of a diode being at r.f. potential elevated from ground, and requires that the biassing feed be isolated to r.f. across the full frequency range covered by the antenna. This is accomplished by groups of r.f.

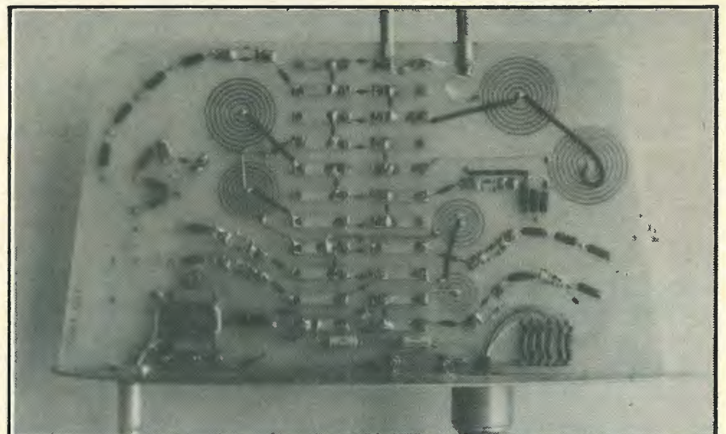


Fig. 5. Unipole version to fit in low-profile shell, covering 30-88 MHz.

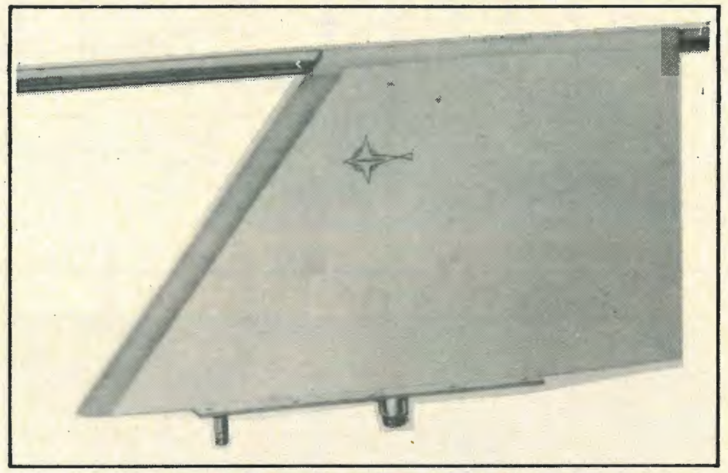


Fig. 6. Broadband u.h.f. and v.h.f. antennas

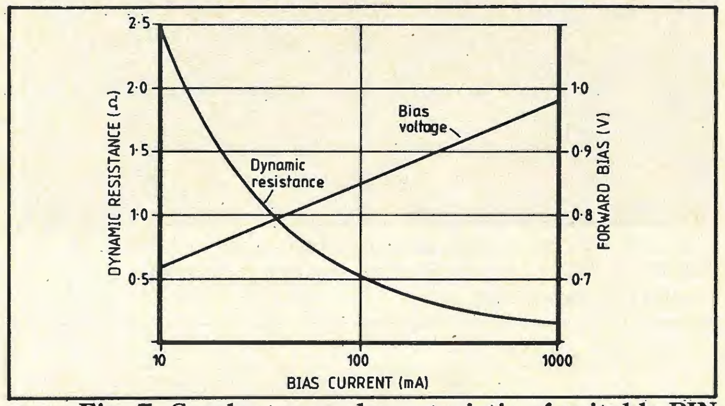



Fig. 7. Conductance characteristic of suitable PIN switching diode.

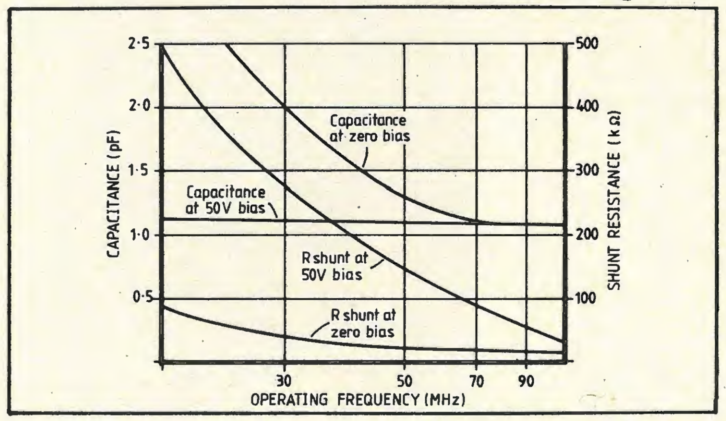



Fig. 8. Capacitance and shunt resistance of diode at varying frequencies, with bias voltage as parameter.

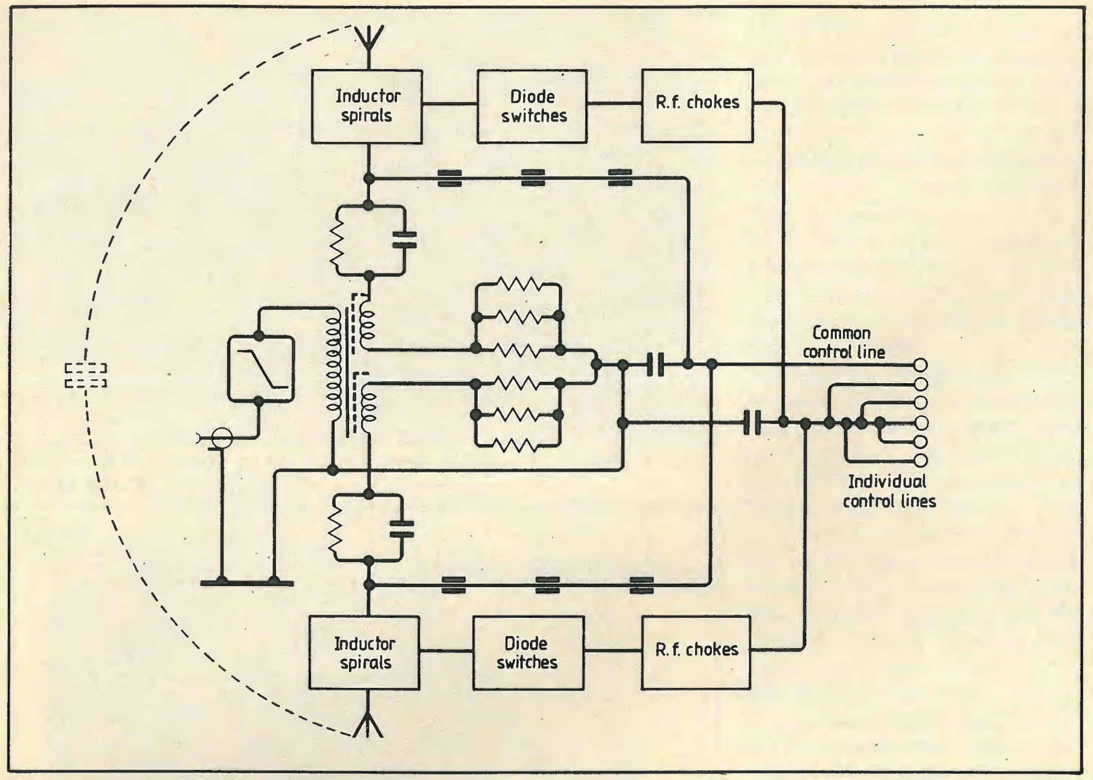



**Fig. 9. Basic bias-feed circuit.**

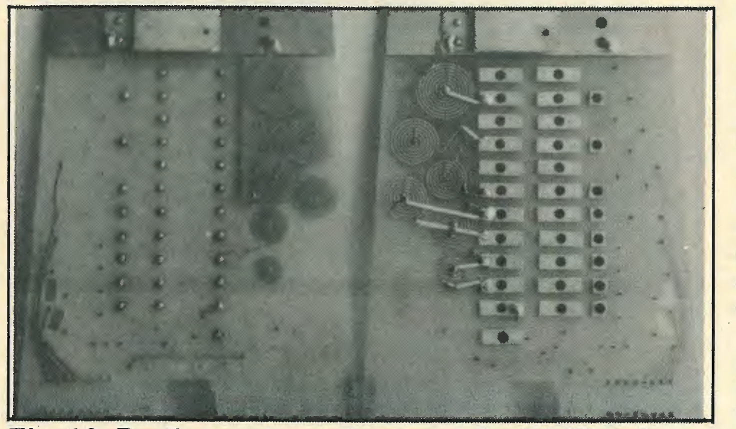
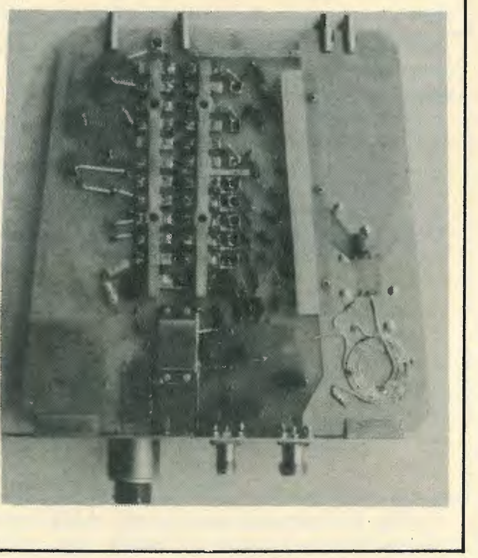


**Fig. 10. Partly constructed antenna for 30-88 and 100-174 MHz bands. Metal coating provides radiating capacitance.**

**Fig. 11. Low/medium frequency version of Fig. 10.**



chokes chosen to have differing self-resonant frequencies, but supplemented (in the reverse-bias state) by use of an isolating diode to feed the inductor-switching diode groups. Figure 9 shows the basic bias-feed circuit, inclusive of a resistor to limit forward-current. The inductor chain provides a common bias-return path, with r.f. and d.c. separated by a further choke group.

Figure 10 shows a partly-constructed tunable antenna covering the low and medium bands 30-88 and 100-174MHz, for housing within the 22cm glass-fibre shell as outlined in Fig. 1(F). The radiating capacitance is provided by silver-coating an area of some 20 square cm on each external face at the top of the shell, with twin interconnections through the glass-fibre walls to the top of the p.c.b. tuning assembly inside the shell.

Figure 11 shows a similar tuning assembly for the low-medium bands, but with the radiating capacitance provided by a length of stainless-steel tubing moulded on the top of the shell, and overlapping it in the aft direction, as outlined in Fig. 1G1/2. Again, twin connections are used for safety. In this design, the p.c.b. is widened sufficiently to accommodate a broadband unipole to one side of the tuning assembly, with u.h.f. radiation assisted by a second, shorter length of tubing spaced from the first by about 4cm. The two sections of this antenna (low-medium bands and u.h.f. band) are coupled to a common terminal via a diplexing combination of low-pass and high-pass filters.

A variant of this design additionally includes printed-circuitry to form a radiator for the IFF band, 1030-1090MHz: when used, this is coupled via coaxial matching circuitry to a separate terminal. As may be supposed, siting of the various metal areas on or attached to the p.c.b. is critical in avoiding their parasitic tendency to create an unacceptable pattern of radiation within the IFF band.

Figure 12 shows the low-band gain or sensitivity of available designs of both tuned and broadbanded antenna forms at various heights, all as measured under substantially identical conditions. Comparisons show, for both forms of antenna, the advantage of height, but more particularly, the considerable advantage of the tuned form as against the broadband form of similar height. Advantage is naturally greatest at the 30MHz extreme, but remains important up to at least the top of this low-band. For antennas of severely restricted height, this diminishing advantage of the tuned form nevertheless remains significant across the medium band 100-174MHz.

It should be remembered that, in the air-to-air mode of communication, the antenna advantage shown will be twice applicable, i.e. during transmission from one communication terminal and during reception at the other, and so can be expected to produce very considerable increase of operational range.

Broadbanded or, more factually, resistively-damped antenna designs provide no selectivity in-band, and usually very little out-of-band, unless supplemented by separate filters. Fig. 13 shows the moderate, but still useful orders of selectivity provided in-band by the tunable antennas. This benefit is made relatively important by the poor spectral purity of typical airborne transmitting equipment, and by the signal frequency pre-selection at the associated receiver.

The two 22cm designs both use a seven-inductor tuning assembly p.c.b., which is double-faced for the three largest inductors, two faces being shown together in Fig. 14. The spirals on opposite faces couple together inductively to provide the required inductance value at best Q, incidentally providing a convenient centre-tap. The other four inductors are printed upon one face only. For six and seven-inductor assemblies shown in Fig.15, the largest inductor $L_6$ or $L_7$ is centre-tapped and switched by eight diodes acting in series across the whole inductor, but bias-fed as four parallel groups each of two series diodes. The smallest inductor $L_1$ is switched by only two diodes acting in series, but bias-fed in parallel. For the seven-inductor unit, the additional isolating diode in each feed line results in up to three diodes in series for bias-feed purposes, each needing a fairly constant 0.85 volt for turn-on. Allowing for some further voltage drop across the resistance of the inductors, a total of some 3.0 volts is the minimum needed for conduction. The bias source provides 5 volts (or 6.5 volts in later units), allowing the limiter resistors in each feed line to have their values set to produce the bias current chosen for individual lines.

Each diode lead terminates upon one of a series of non-grounded heat-sink plate, with lead lengths cut as short as practicable to minimize both temperature differential plate-to-diode, and the stray inductance which, with all diodes conductive, limits the upper frequency of operation.

Each bias feed line is individually filtered against (principally) transfer of transmission r.f. back into the bias source and its information-decoding circuitry. In current designs, this filtering uses ferrite beads and by-pass capacitors, the values of these latter, in association with the output resistance of the bias source, being the limiting factor in switching speeds for any given decoder characteristics.

Matching must be effected between the usual 50 ohm line and the impedance of the series-tuned radiating circuit. Although $R_r$ will be a significant part of this impedance, the objective is for maximum transfer between line and circuit, and matching must therefore be to the total $R_t$ of $R_r$ and the various sources of loss resistance $R_1$. This latter is principally due to the imperfect conductivity of the diodes when forward-biased and to the losses of the tuning inductors. Power-efficiency of the radiator circuit is then related to the ratio $R_r$ to $R_t$, and is similar, though not identical, for the transmission and reception functions.

The losses $R_1$ can change appreciably for quite minor changes in frequency setting. Up to about 38MHz, the largest inductor $L_6$ or $L_7$ is always in circuit. At 39MHz, it is removed, thereby substituting the resistance of the eight diodes used to short-circuit it, but then bringing into circuit all or most of the five or six smaller inductors, which coincidentally removes the losses of up to 16 diodes. However, the inherent losses of $L_6$ or $L_7$ will be considerably lower than for the total of the group $L_{1\text{-}15}$ or $L_{1\text{-}6}$ as producing almost the same inductance value, hence tending to offset the effects of diode losses and so maintain overall losses sensibly constant. Although early designs incorporated diode-switching of the matching ratio, careful manipulation of the balance between different loss-sources has allowed use of only a single matching ratio across the whole of the 30-88MHz band.

Matching is accomplished through a ferrite-cored auto-transformer. Core material found to be most suitable for the 30-88 band becomes appreciably lossy at the upper extreme of the 100-174 band, and might better be substituted by an alternative form of matching, e.g. a capacitor network. However, in trials to date, the advantage was nullified by losses in the additional switching network needed, and the ferrite transformer is currently used for matching across the full bands 30-174MHz.

Switching-bias is provided in a separate unit, powered from the aircraft's 28 volt d.c. line, and which includes the logic or code conversion circuitry. Frequency-setting at the transceiver originates as any of several different serial or parallel data codes, which must be converted to the near-binary code required for antenna con-

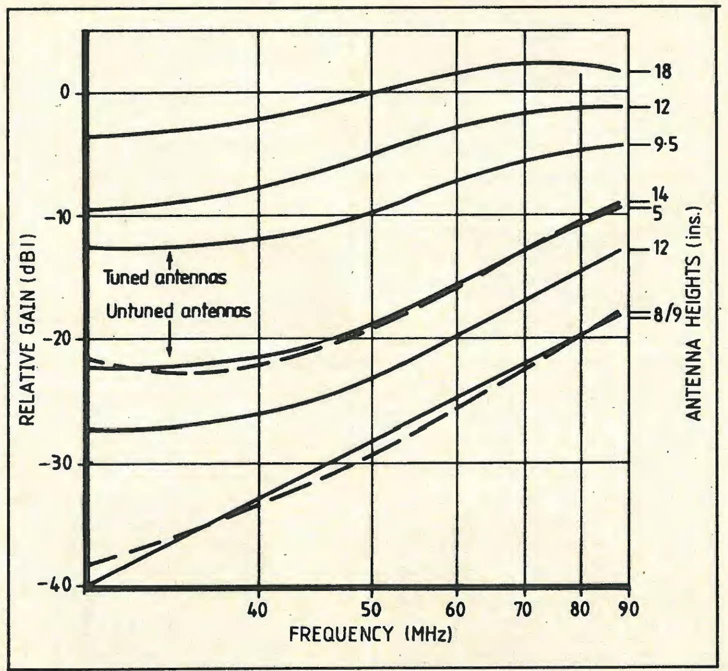



**Fig. 12. Gain or sensitivity of tuned and untuned antennas.**

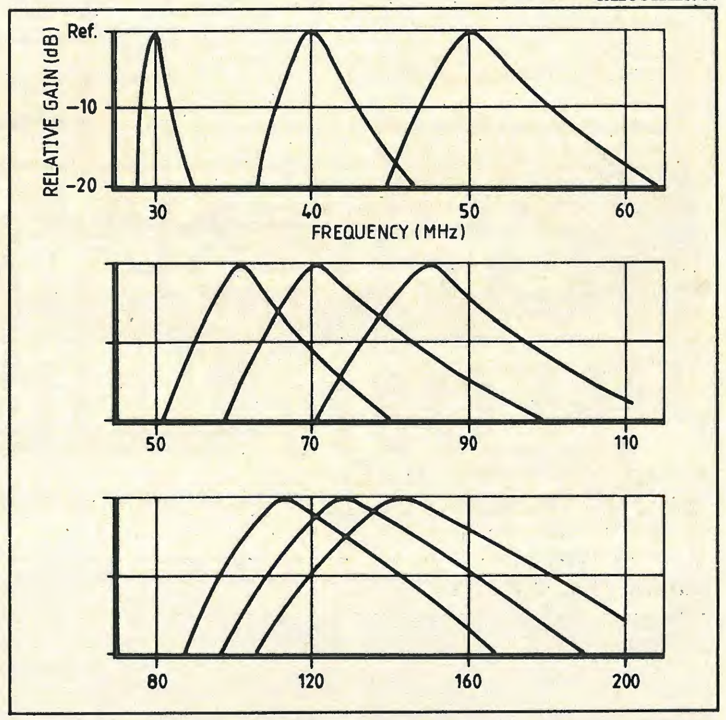



**Fig. 13. Some useful selectivity is provided, in-band, by tunable antennas.**

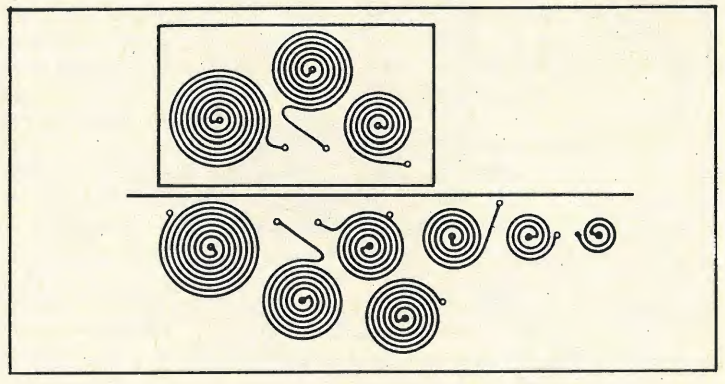


**Fig. 14. Inductor printed-board assembly.**

trol. In the case of serial-data code, a single line encircling the aircraft carries data for numerous different items of equipment, and the antenna code-converter must include the facility to recognise and act upon only the applicable information. It also includes facilities to avoid loading the data line, even under fault conditions.

In present units, turn-off bias (positive to ground) derives directly from the 28 volt line, after filtering. Turn-on bias derives through a d.c.-to-d.c. converter, providing 5 volts stabilised for up to about 1 ampere current. In later units, both bias outputs are derived through converters, the turn-off supply being increased to about 60 volts (at negligible current) and the turn-on supply increased to 6½ volts, stabilised for up to 1½ amperes. Both these increases are directed at improving either or both of power rating and harmonic generation.

The turn-off bias is permanently applied to the antenna diodes via relatively high-resistance feed paths, and can therefore be over-ridden by turn-on bias applied through low-resistance paths.

All the antenna designs described in this article are already in service in varying quantities, but the basis of tunable design is being extensively developed for further applications, whether frequency-hopping or otherwise, particularly in connection with suppression into the airframe contours.

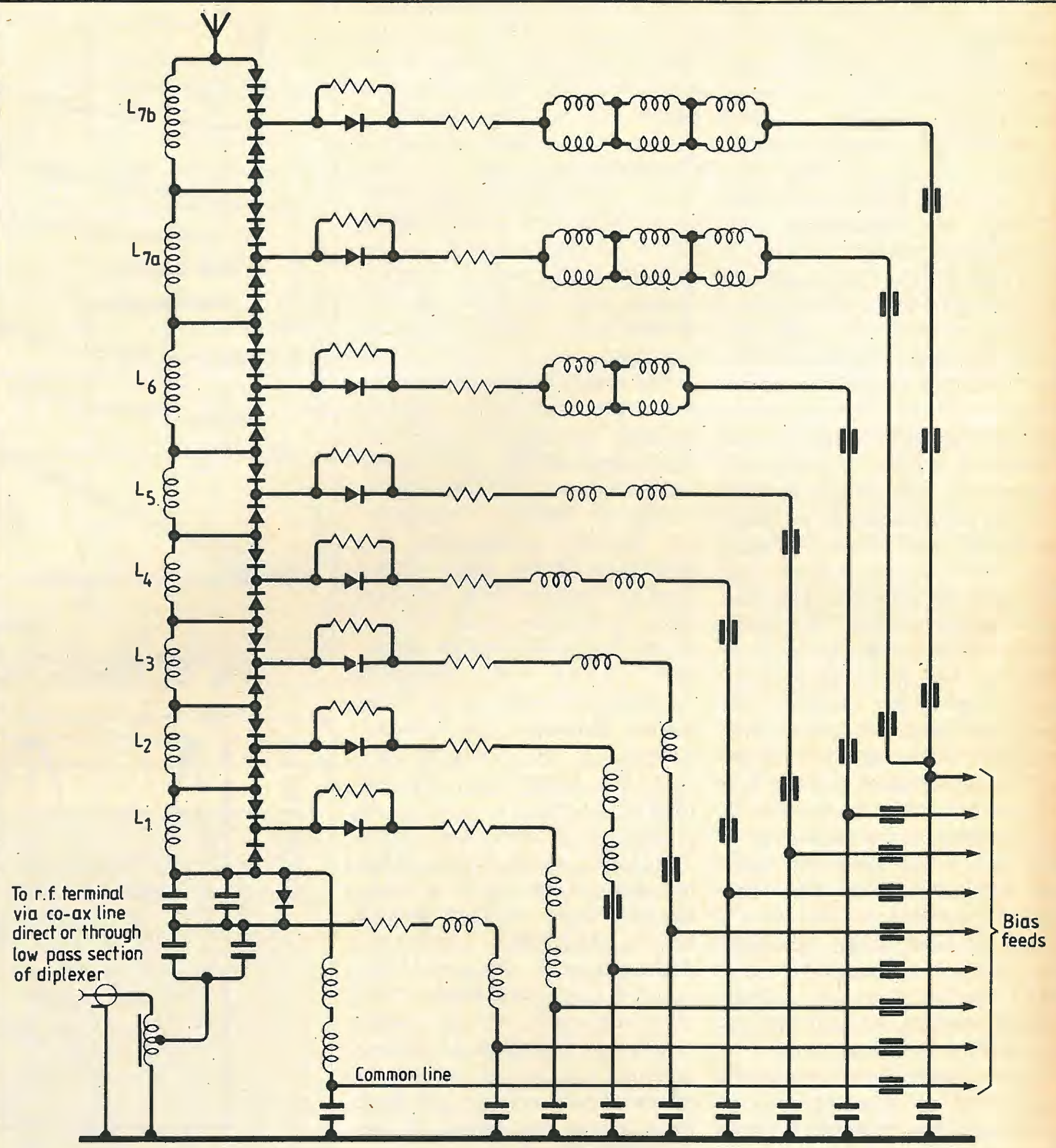



**Fig. 15. Circuit of seven-inductor antenna tuning assembly.**

## Breaking into print

The Editor always welcomes contributions from readers; and a quick and easy way to send them is via our Beeline computer. But there is no need to bludgeon your way in, like the unsuccessful hacker who showed up (right) in our system log recently.

The routine is very straightforward. All you need is a terminal and a 300 bit/s V.21 modem: the data word length is seven bits plus an even parity-bit and one stop-bit. Dial the number (01-661 8978 or 01-661 8986), type EWW in capital letters (the address code for *Electronics and Wireless World*), press <return>, wait for the system to respond with

+++ STF GO

and send your message. Sign off with a carriage-return and NNNN, also in capital letters, and make a note of the code number the system returns you — it will help us trace your message if anything goes wrong. Then ring off.

Your message should consist of plain Ascii text and can include lower-case letters as well as upper-case. Make sure that it states clearly at the top who it is for; otherwise it may end up in the *Practical Toadbreeding* office. The text will be printed out on a continuous roll of paper and so you may wish to provide your own pagination. A spooled text file from a word-processor is very suitable.

Since the page-width of our printer is 69 characters (the standard for telex) your line-length should not exceed this. Carriage-return characters must be accompanied by line-feeds, but the escape code (Ascii 27) and most other control characters should be avoided; Beeline will suppress them.

However, the system does support Xon-Xoff flow control. So if you receive our carrier tone but get no response when you type EWW, try waking the port up by sending control-Q and start again.

```
READ  -215-  -012-  -012- +++ ? ERROR  -012-  -215-  -012-
WRITE CMD:1 -215-
READ  -215-  -012-  -012- +++ ? ERROR  -012-  -215-  -012-
WRITE : -215-
READ  -215-  -012-  -012- +++ ? ERROR  -012-  -215-  -012-
WRITE STF -215-
READ  -215-  -012-  -012- +++ ? ERROR  -012-  -215-  -012-
WRITE SCF -215-
READ  -215-  -012-  -012- +++ ? ERROR  -012-  -215-  -012-
WRITE START -215- 4
READ  -215-  -012-  -012- +++ ? ERROR  -012-  -215-  -012-
WRITE START -215-
READ  -215-  -012-  -012- +++ ? ERROR  -012-  -215-  -012-
WRITE GO -215-
READ  -215-  -012-  -012- +++ ? ERROR  -012-  -215-  -012-
WRITE PAGE -215-
READ  -215-  -012-  -012- +++ ? ERROR  -012-  -215-  -012-
WRITE HELP -215-
READ  -215-  -012-  -012- +++ ? ERROR  -012-  -215-  -012-
WRITE +++ ? ERROR -215-  -215- A1 -215-
READ  -215-  -012-  -012= +++ ? ERROR  -012-  -215-  -012-
WRITE SYSTAT -215-
READ  -215-  -012-  -012- +++ ? ERROR  -012-  -215-  -012-
WRITE SYSTEM ACCESS NUMBER 2 ACCESS DENIED -215-
```

# Data conversion

## An introduction to analogue-to-digital and digital-to-analogue conversion.

Digital processing power has greatly increased over the past decade. In the latter part of 1985, Inmos Intel, Motorola and National Semiconductor all announced new or upgraded processors.

Domestic digital video and audio playback machines are now readily available and digital techniques are used in much of the broadcast chain. On the instrumentation side, digital-storage oscilloscopes are becoming cheaper because of falling i.c. prices, and digital meters are commonplace.

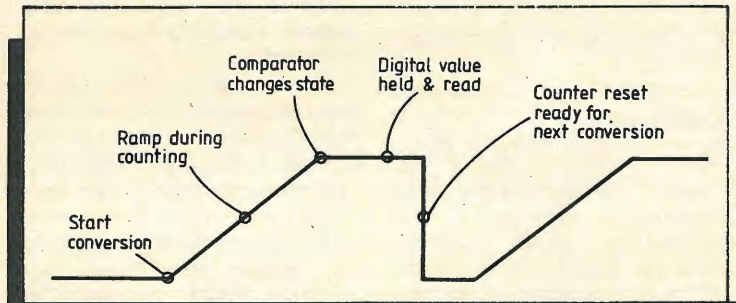
These advances in digital processing are calling for more diversity in the types of converter available — and for lower prices. Faster processors with wide data buses mean the production of more fast, high-resolution converters with microprocessor compatible inputs and outputs. Already there are devices that connect directly to a linear circuit at one end and to a microprocessor bus at the other with little more than address-decoding.

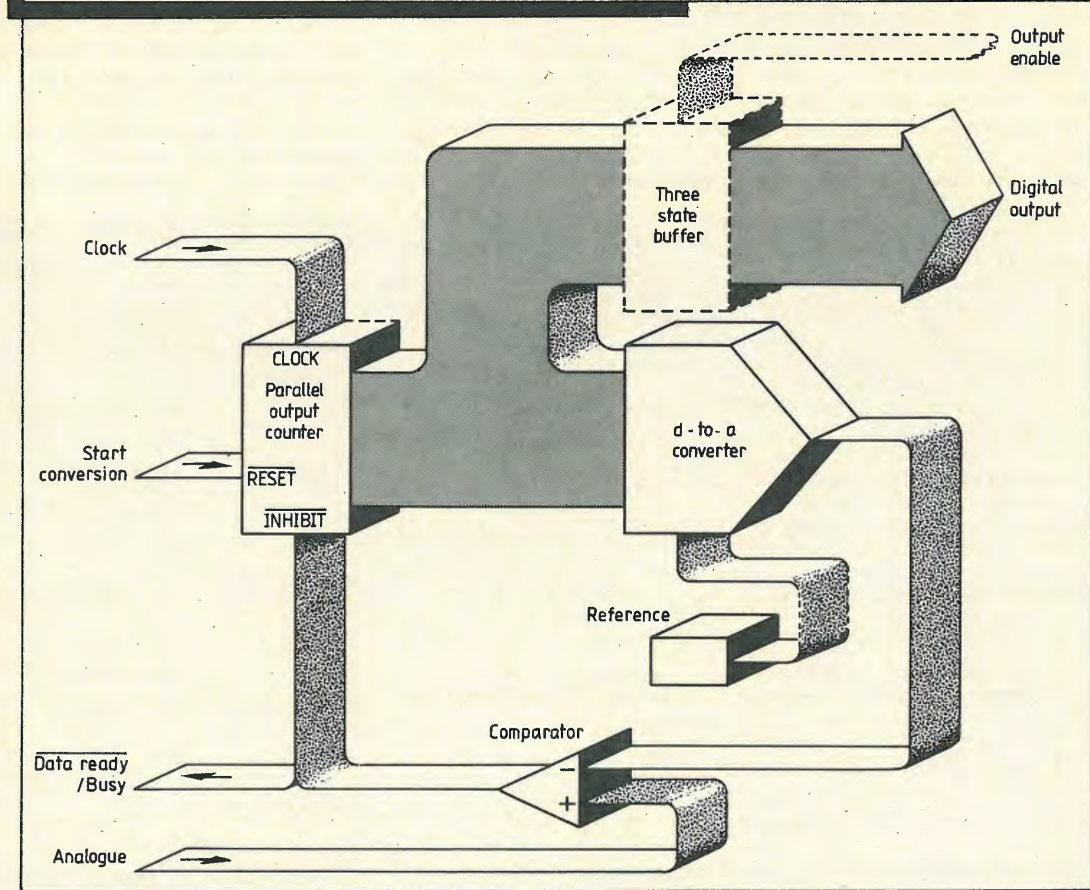
Progress in digital audio and video has led to the design of special purpose converters. These include video converters with 75Ω output and sync. inputs, and fast audio converters with high resolution and low t.h.d. New and improved i.c. manufacturing processes have allowed the production of microprocessors and controllers with on-chip converters, and monolithic digital meter i.cs with linear inputs and display driver outputs.

Fast and accurate data converters have been available for many years in the form of expensive hybrid devices or circuit boards full of i.cs. Cheaper monolithic converters have typically had lower accuracy and needed external circuits for buffering, references, data latches, clocking, etc.

But despite the problems of manufacturing high-speed digital circuits and high-accuracy linear elements on the same chip, there are now many complete monolithic converters being produced for a few pounds that are equal to or better than older hybrids and modular products. This doesn't mean a decline in hybrid circuit sales though; hybrid manufacturers have simply advanced their products to a point where monolithic devices cannot yet compete.

In the future, we will see many more general-purpose computers with analogue inputs and outputs, particularly for instrumentation applications. Provided that they are fast enough, such computers could perform every imaginable instrumentation task — waveform analysis and synthesizing, amplification, sensor reading, frequency counting, voltage measurement, etc. — and all with the advantage of digital storage and flexible data processing.




**Simplified ramp-type a-to-d converter. Main elements in most a-to-d converters are a d-to-a converter and comparator. Ramp types are simple and can be as accurate as any other type but conversion time is variable and relatively slow. Even with a relatively low resolution eight-bit converter, it takes 255 clock pulses before the d-to-a converter output is ramped up to the maximum analogue input voltage. Lower input voltages require fewer steps. The waveform is output from the d-to-a converter.**

## D-to-a conversion

Nearly all digital-to-analogue converters work in the same way. A digital value, usually in the form of a parallel binary data word, is presented to a resistor network through a set of switches and a proportional current flows at the network output.

For some applications, a data latch and discrete resistor network suffice. Unless the converter is being used to turn static digital data into analogue form, as it would be if say thumbwheel switches were presenting the data, latching is essential. Many converters now include latching circuits.

Another important point is that current output from the resistor network is relatively high impedance. A buffered voltage output is more useful in most applications and again, many d-to-a converters have on-chip output buffering. Integral current-to-voltage converters increase settling time of the converter though.

Accurate converters need an accurate reference voltage. Often, the converter has an independent built-in reference with its own output, and a separate reference input is available. Normally, the output is connected directly to the converter reference input but, in a multiplying converter, the internal reference output can be disconnected and an external varying reference can be connected to the reference input instead.

Multiplying converters allow analogue output to be proportional to the product of the reference and the fractional equivalent of the digital input value, acting as a sort of digital potentiometer. If a number of converters are used together, reference output from one converter may be used to feed others to give good tracking.

Enhancements to the basic d-to-a converter take many forms. Adding sample-and-hold circuits to the output of an accurate d-to-a converter gives multiple channels. There are converters with gated outputs for frequency and time-division multiplexing and there are logarithmic output and multiplexed data input devices for high resolution using narrow data buses. Some converters even include a shift register so that data may be fed in serially. Precisely matched multiple converters on a single chip can also be found.

## A-to-d converters

Many analogue-to-digital converters include a digital-to-analogue converter and comparator. The unknown analogue signal feeds one input of the comparator and analogue output from the d-to-a converter feeds the other. Level of the unknown signal is determined by sending digital values to the d-to-a converter and looking for a change in state at the comparator output. At this change of state, the digital value at the d-to-a converter output represents the analogue input value.

Where speed is not important, sequentially incrementing digital values starting from zero are sent to the d-to-a converter. If the input voltage is high, hundreds of values may need to be sent to the d-to-a converter before the comparator switches. With an eight bit converter, the number of values sent can be as high as 255 for maximum input voltage. Some a-to-d converters include a counter and are very useful for generating ramp outputs.

For faster applications, a little logic is used. The first value sent to the d-to-a converter is half way up the scale, i.e. the most-significant bit only of the d-to-a converter is switched on. Comparator output is checked for a higher or lower indication; if higher, the bit is left on. The next bit is now switched and the same check done, and so on down to the l.s.b.

This technique, successive approximation, reduces the number of steps required to the number of bytes in the word. Again, many converters include successive approximation registers and require only an accurate clock signal. Alternatively the successive approximation can be done in software under computer control.

Tracking converters use comparator output to control whether the counter driving the d-to-a converter counts up or down. As the name implies, output from the d-to-a converter tracks the analogue input so that after an initial count up at switch on, digital output is always true.

Voltage-to-time type a-to-d converters are an alternative for slower applications. With this type of converter, the number of bits of resolution is not dependent on accuracy of a resistor network but on charging of a capacitor. Noise rejection is also inherent provided that sample and hold circuits are not used at the input.

In its simplest form, this type of converter consists of a resistor and capacitor connected to a comparator input, and a counter driven by an accurate frequency clock. A reference voltage is connected to the comparator's second input.

Before the conversion, the capacitor is discharged and the counter reset. At the start of the conversion, unknown input voltage is allowed to charge the capacitor through the resistor and at the same instant the counter is started. When the capacitor voltage reaches the reference threshold, the comparator output switches and clock is stopped. The counter now holds a value representing the time it took to charge the capacitor.

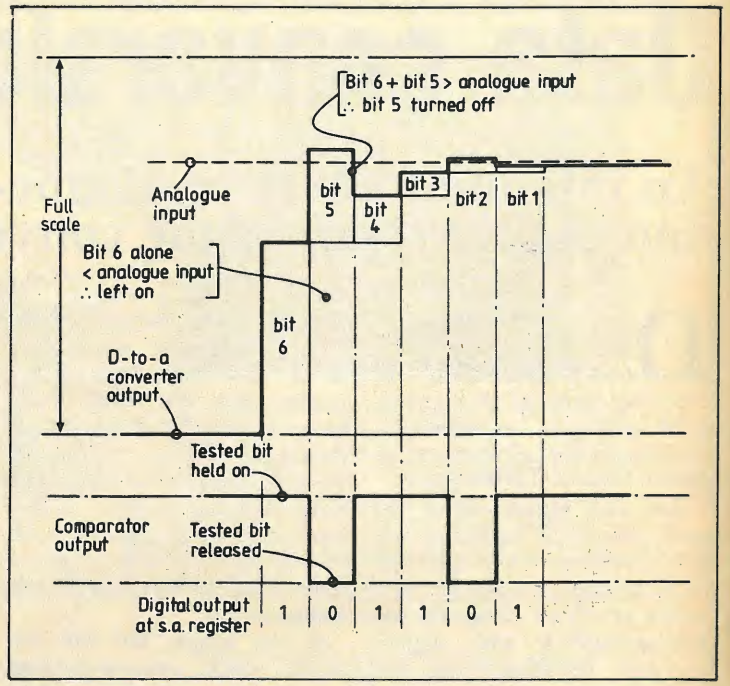
With this crude form of voltage-to-time converter, the voltage representation on the counter is not linearly proportional to the input because of the capacitor charging curve so interpretation is necessary. Voltage input must also be higher than the reference.

Practical voltage-to-time converters use an op-amp integrator at the input and semiconductor switches. In a dual-slope integrating converter, current proportional to the input voltage charges the integrator capacitor for a fixed number of clock periods. The counter is then set back to zero and used to count the number of clock periods taken to discharge the capacitor to the starting point using an opposite polarity current proportional to the reference. Discharge time is thus directly proportional to the average input signal value.

Sometimes a third operation is included to compensate for errors at the integrating amplifier input. Charging the capacitor with zero input gives a drift error which can be inverted and used as a compensation value to be introduced when integration of the input signal occurs. Such integrating converters are called triple or quad-slope converters.

Fastest a-to-d conversion is obtained by using a resistor network and many comparators. Such converters, referred to as parallel or flash types, are used in video, radar and instrumentation applications.

They are fast because there is only one step in determining the input voltage. But to do so they need $2^n$-1 comparators and divider taps, where n is the number of bits in the digital word, and a proportionally large amount of priority-encoding logic. A compromise is the subranging converter which processes the digital word in two parts.




**Successive approximation used in a-to-d converters speeds up conversion time. Elements of this type of converter are similar to those of a ramp type but the counter is replaced with a successive approximation register. The number of conversion steps required is equal to the number of bits in the data word as this example for six-bit conversion shows.**

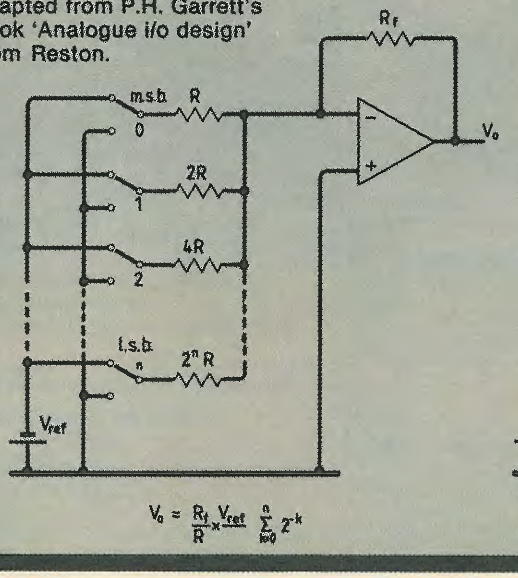
### Converter networks

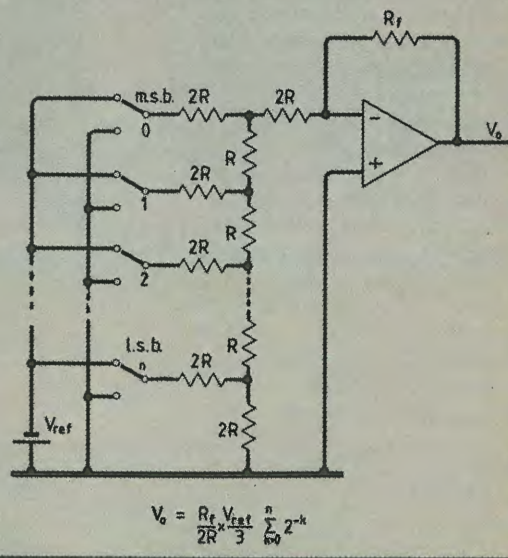
In a weighted-resistor network, current is halved in each bit step toward the l.s.b., by doubling the value of resistance R. Current from each stage is summed to give an anologue output.

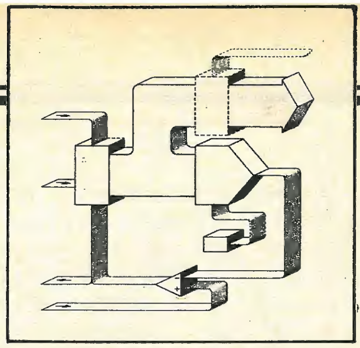
This method is simple but not often used because many different resistor values are needed and values become very high as the number of conversion bits increases. With a value of R = 1kΩ in a 12bit converter, the l.s.b. resistance value is over 2MΩ. In a converter using discrete resistors, finding the required values is also a problem.

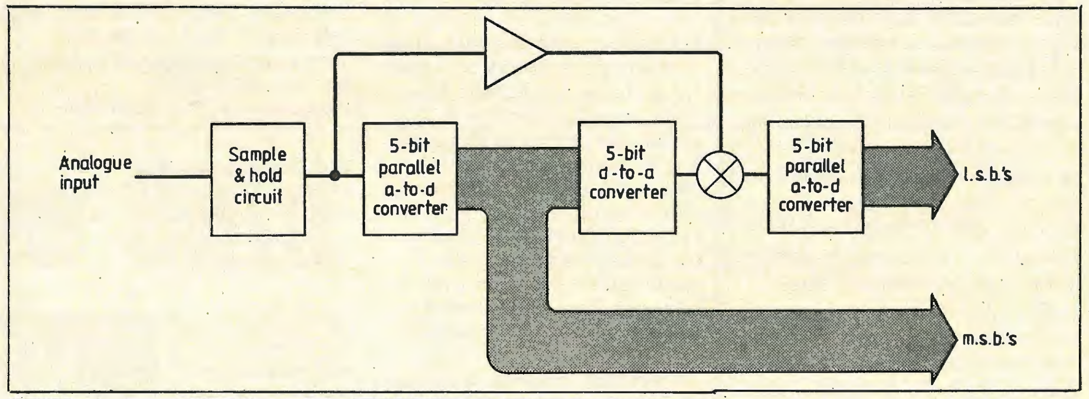
Only two resistance values are required in the R-2R ladder network, regardless of the number of conversion bits. Current from each stage output is divided by the ladder network.

These diagrams are adapted from P.H. Garrett's book 'Analogue i/o design' from Reston.

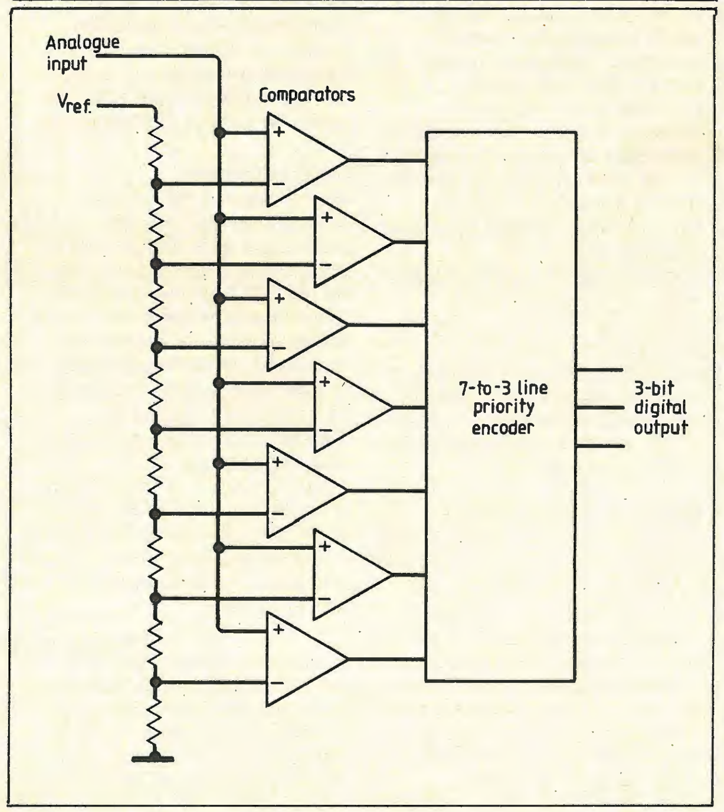





**Subranging converters use two lower resolution parallel a-to-d converters and a d-to-a converter to combine high resolution with speed.**




**Parallel or flash a-to-d conversion is fast but requires many components and complex encoding — as this example for only 3bit conversion shows. As a result, high resolution flash converters become expensive. Most are 6-8bit devices.**

As with d-to-a converters, a-to-d devices might have a separate input for reference voltage to allow ratiometric conversion. This might be used for example in bridge-circuit type measurements where the internal reference would be replaced by one derived from the reference feeding an arm of the bridge.

Sample and hold circuits can be applied at the input of almost any type of a-to-d converter to give multiple channels.

#### Tips for choosing a converter

Cost, accuracy and speed are primary factors in choosing a converter but completeness is also important. Errors such as temperature and long-term drift might need to be considered, as might setting up complexity.

Digital input or output data levels are usually t.t.l. compatible but that does not always mean c-mos compatible. Some fast converters are e.c.l. compatible. Parallel data on higher resolution converters may need to be accessed or presented in two parts. This is the case with say a 12bit converter designed for use on an 8bit data bus. Using such a converter with a 16bit data bus wastes time.

Resolution does not necessarily go hand-in-hand with the number of bits in the data word. Zero, gain, linearity and differential linearity errors all contribute to overall accuracy.

In a d-to-a converter, useful features are an internal reference, input data latches, and output buffering. Many converters can now operate from a single supply rail and give voltage rather than current output.

Because of the number of types available, choosing an a-to-d converter is not so straightforward. In some simple a-to-d converters, a ramp counter is used but it is not accessible so clock pulses need to be counted externally. For other than computer applications, either choose a successive approximation converter or make sure that the counter is accessible.

With the exception of parallel converters, most a-to-d converter need an accurate clock signal. Three-state digital outputs are essential for connection to a microprocessor bus. High input impedance might be required, in which case a c-mos converter is the obvious choice.

## Converter terms

**Band-gap reference.** A reference voltage derived from the predictable base-emitter voltage of a silicon transistor.

**Bipolar.** Sometimes analogue signals that may be either positive or negative need to be processed. Converters for doing this are called bipolar. The term is also used to describe converter i.cs using bipolar transistors as opposed to, say, mos devices.

**Charge-balancing converter.** This is an integrating a-to-d converter in which charge placed on a capacitor by the analogue input is balanced out in the integrator by pulses of reference current. Balancing of the voltage involves averaging over the measurement period. Charge balancing is also called quantized feedback.

**Conversion rate.** Normally this is the reciprocal of time taken for a converter to make its worst-case conversion to within the specified accuracy but in some high-speed devices, a new conversion starts before the old one has finished (pipelining). Worst-case conversion usually occurs when the converter changes from its highest to lowest value and *vice-versa.*

**Differential linearity.** A change of any one l.s.b. in digital value represents a given change in analogue voltage or current. The difference between this change in practice and the ideal one of full-scale range divided by two to the power of the number of bits in the digital word is referred to as differential non-linearity error. This specification relates to step size, not to errors in the overall curve produced when stepping the converter through all digital values; see integral non-linearity. If any two steps differ by more than 1 l.s.b., the converter could be non-monotonic.

**Dual-slope converter.** For analogue-to-digital conversion, the unknown analogue voltage or current may be converted into a time period using an integrator and reference. This period is represented by the digital value at a clock-pulse counter, which is first used to take a fixed-time sample of input, then to compare the sample with time taken to discharge the integrating capacitor by an equal amount using an opposite reference current. Clocking and counting may be done within the converter or under computer control. Dual-slope conversion is slow but can be very accurate.

**Flash converter.** As the name implies, these converters are usually fast, converting an analogue value to a digital word in one step. Analogue input feeds many comparators ($2^n$-1, where n is the number of bits in the digital word), each with a different reference value. All comparators with reference below the analogue input voltage change state (or comparators above the reference depending on construction of the device) and the comparator outputs feed priority-encoding logic to convert to binary or any other desired code. Because they use many comparators and references, flash convertors with a large number of output bits are difficult to manufacture and expensive.

**Full-scale range.** For conversion in either direction, f.s.r. is the difference between maximum and minimum analogue values.

**Gain error.** Sometimes called full-scale error, this figure expresses the difference between actual and ideal converter transfer-function slopes. In d-to-a converters, it might be possible to compensate for gain and zero errors in output buffering.

**Integral linearity.** Specifications for integral linearity, which may be expressed as a percentage or as an l.s.b. fraction, give you an idea of how the converter responds over the whole of its range. This error is the maximum deviation between the curve of values produced by stepping a converter through the whole of its range and the ideal curve. A converter with no differential-linearity error may still have an integral-linearity error. Gain and zero errors are not necessarily included in the error figure.

**Integrating converter.** Dual-slope and charge-balancing a-to-d converters fall under this heading, which describes a device in which analogue input is integrated with time.

**Linearity error.** See integral and differential linearity.

**Major transition.** When the most-significant bit of a converter changes to one and all other bits are zero, or *vice-versa,* the event is described as a major transition. Maximum linearity error usually occurs at the major transition, since the m.s.b. has the largest error as a percentage of full scale.

**Monotonicity.** If an increment of any one l.s.b. in a d-to-a converter produces an increase in analogue output, the converter is said to be monotonic. Differential linearity errors exceeding ± 1l.s.b. and/or integral-linearity error outside ± 1/2l.s.b. may result in non-monotonicity.

**Multiplying converter.** D-to-a converters with a reference voltage input that can be used with a varying reference are referred to as multiplying converters. Output is proportional to the product of the reference and the fractional equivalent of the digital input number.

**Parallel converter.** (See flash a-to-d converter).

**Quad-to-slope conversion.** An integrating converter using two cycles of dual-slope conversion is a quad-slope converter. This technique enhances accuracy. One cycle uses a zero input and the second the analogue input. Errors from the first conversion are subtracted from the first.

**Ramp converter.** In this method of analogue-to-digital conversion, inputs of a comparator are fed by output from a d-to-a converter and the unknown analogue input. Digital values for the d-to-a converter come from a counter driven sequentially by a clock. Output from the d-to-a converter is thus an analogue ramp. When ramp voltage is equal to the analogue input voltage, the comparator changes state and the digital value is read directly from the counter. An enhancement to this method is successive approximation which greatly reduces the number of values presented to the d-to-a converter.

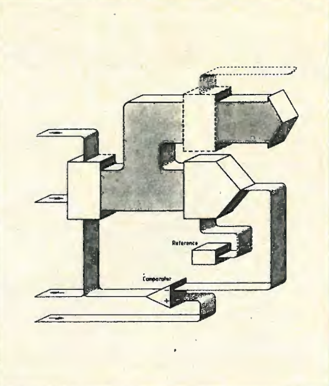
**Ratiometric conversion.** Mainly, a-to-d converters are required to read absolute values and they do so using a fixed reference. Occasionally, say when a bridge measurement circuit is being used, it is better to apply an external reference. In the case of a bridge measurement circuit, the reference would be derived from the bridge reference to give more accurate results. This is ratiometric conversion.

**Resolution.** For an a-to-d converter, this term is used to express the smallest analogue change that the converter can resolve. For a d-to-a converter, it is the change in output voltage for a one l.s.b. change in input. Resolution is usually given as the number of bits in the digital word. An ideal eight-bit converter for example resolves to 1/255 (or $1/(2^8-1)$) of the full-scale input or output.

**Settling time.** Usually specified for a change in digital input from all zeros to all ones or *vice-versa,* settling time is the time taken for output of a d-to-a converter to settle within a given tolerance band after a change in input.

**Subranging converter.** Very fast and accurate analogue-to-digital converters can be made by converting the digital word in two or more parts using flash converters. In a subranging converter, the most-significant part of the output word is digitized then converted to an analogue voltage. This analogue voltage is fed back and subtracted from the input to get the digital value of the least-significant part of the word. Finally, the most and least-significant values are combined. Some converters include correction for the least-significant bit of the most-significant word portion. Using a single flash converter to convert the whole word would be impractical or too expensive because of the number of comparators, ladder resistors and associated priority encoding logic.

**Successive approximation.** This technique reduces conversion time in analogue-to-digital converters using a resistor-network d-to-a converter and comparator (see ramp converter). Rather than stepping the d-to-a converter through all of its values sequentially to see when the comparator output changes state, the d-to-a converter is first fed with a value equal to half of its full scale by switching the most-significant data bit. Comparator output is checked. If the comparator indicates that the input voltage is higher than half way up the scale, the m.s.b. is left on; if the input is lower, the bit is switched off. The same is done for the next most significant bit and so on until the l.s.b. In this way, for an eight-bit converter say, the analogue input value can be found in eight steps rather than in anywhere up to $2^8$. Some monolithic and hybrid converters have successive-approximation circuits on-chip, usually requiring an external clock signal, but successive approximation can be easily carried out by computer at the expense of processing time.



**Tracking converter.** This type of converter is similar to the ramp converter but instead of the counter being ramped directly by a clock signal, it is incremented or decremented depending on output from the comparator. Output from the d-to-a converter thus follows the analogue and as a result, digital output from the converter always represents the analogue input. Tracking allows low-frequency signals to be digitized without using a sample-and-hold circuit.

# Trends in data conversion

Mark Riley, B.Sc. Ph.D. Analog Devices

Data converters currently represent some 23% of linear i.c. sales and growth over the next five years is expected to average 25%. Mark Riley talks about the evolution and future of data conversion in one of the leading companies.

Ten years ago, designers perceived data conversion as an unfortunate by-product of microprocessors and few were capable of applying the technology. Since then, design expertise and technological advances have been combined to produced much simpler and cheaper solutions to the problem of data conversion.

Over ten years ago, the first monolithic 10 bit d-to-a converter heralded the demise of the traditional modular or hybrid approach and gave rise to a range of integrated circuit a-to-d, d-to-a, v-to-f, f-to-v and synchro-to-digital converters.

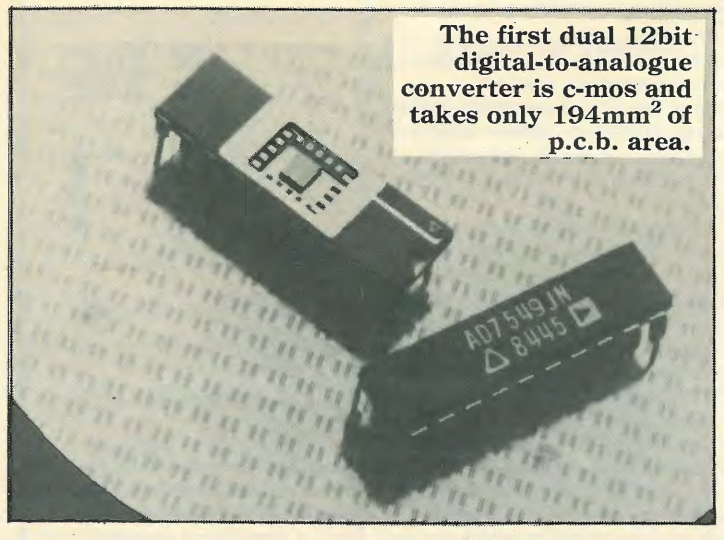
Subsequent monolithic product developments have centered on two complementary technologies — bipolar for high speed complete devices and c-mos for medium-speed building block type applications and low-power consumption.

#### Bipolar evolution

The first monolithic precision d-to-a converter that required no user trimming used a straightforward 7μm n-well bipolar process but pioneered the introduction of on-chip laser trimmed thin-film resistors and stable buried references.

Geometry reductions to 5μm and refinements of this fundamental technology have subsequently yielded higher resolution d-to-a converters with features such as output buffers. For example a typical microprocessor interfacing 12 bit device with 3μs conversion time and output buffer is now available in plastic dip packaging for under £10.

Monolithic precision a-to-d converters using bipolar technology started with the



**The first dual 12bit digital-to-analogue converter is c-mos and takes only 194mm² of p.c.b. area.**

introduction of a 10bit successive approximation device using integrated-injection logic for the approximation function. The same technology and an enhancement in laser trimming has recently resulted in a complete 12bit a-to-d converter that could previously only be produced as a two-chip hybrid device.

Faster 10MHz microprocessors and speed limitations of integrated-injection logic indicate the need for better and finer-geometry processes to allow fast low-power devices with temperature-stable linear cells and faster logic switches.

Bimos II is a new n-well bipolar/mos process optimised for n-p-n linear capability by deep diffusion in the n-well. It uses two-layer metalization. An initial product using this technique is a monolithic 16bit d-to-a converter with input latches and buffered output. Employing fast current-steering switches, this 12mW device takes only 6µs to settle to within 0.001% for a 10V step while maintaining monotonicity over its 16bit range.

Within the next 12 months, this process is to be used to produce a new family of monolithic converters with settling and conversion times of orders of magnitude better than is presently possible and with bus architectures entirely compatible with the latest generation of microprocessors.

## Developments in c-mos

We manufactured our first c-mos devices in 1973 using an adopted 10µm p-well process. In refining this process, important problems such as latch-up suppression, accuracy and reliability were addressed and solved.

On solving one of the main problems — that of producing a 12bit accuracy comparator — it became possible for the first time to fabricate a true 12bit successive approximation a-to-d converter in c-mos. Further refinements have recently led to production of the most accurate 12bit a-to-d converter with an error of just ¼ l.s.b.

To accommodate precision linear components on the cmos chip, a proprietary 15V linear-compatible c-mos technology was developed. This all ion-implanted 4µm process uses self-aligned polysilicon gates. It allows highly stable mosfet devices and high-performance p-n-p bipolar transistors to be fabricated on the same chip. The p-n-p devices give low input noise.

Manufacture of the first 12bit c-mos d-to-a converter with voltage output was made possible by this process. Further refinements and shrinking of the process now provide 5V operation at high speed but more importantly the p-n-p structure allows on-chip bandgap references to be built into complete d-to-a and a-to-d converters.

Soon to be announced is a 12 bit 5µs a-to-d converter made using this process with 50ns bus access time, on-chip reference and clock, single-supply operation and 120mW power consumption. A voltage-output d-to-a converter with on-chip reference and double buffering will be available within the next few weeks.

## Sales and innovation

Customer demands for data conversion are to some extent initiated by the innovation of converter manufacturers. In other words, converter sales areas are being created by the supplier anticipating rather than reacting to customer demands. It is the rapid development of appreciated technology that has led to new product concepts and lower prices.

An ever increasing number of functions in the converter circuit is demonstrated by the fact that the first 10bit d-to-a converter occupied a chip area of four tenths that of a current 16bit d-to-a converter with two-layer metalization.

Ability to manufacture substantially larger die on progressively larger wafers (3in to 6in) together with integration of the hitherto external chip functions give the customer what is wanted — many functions, low cost, low power, small size and high speed.

An important factor of having solved the problem of manufacturing functionally complete data conversion devices with no user trimming at 10 and 12bit levels is the affect that it is beginning to have on 8bit devices. These traditionally low-cost devices are far more significant in that they are sold in large numbers.

Users of 8bit devices are finding that much of the cost of using these cheap devices is in trimming and setting up. Consequently the need for devices that can be used without setting up is increasing. Surface mounting techniques are placing similar demands on converter manufacture. Reduction in the size of the overall system board makes it practically difficult to use set-up trimmers.

## Will converter sales decline?

There is an unwritten assumption that the need for data conversion devices will decline as microprocessor manufacturers incorporate on-chip signal-processing circuits, and as the use of digital audio, tv and automobile electronics increases.

The fact remains that by incorporating a-to-d converters in a microprocessor, potential applications for such a product become limited by dynamic and resolution considerations of the converter.

Digital audio has indeed caused the production of 16bit d-to-a converters with appropriate t.h.d. specifications but these cannot cope with the monotonicity that might be required in a closed loop control system. Digital tv manufacturers have pushed forward flash-conversion but only for a specific signal bandwidth.

Converter design-to-manufacture time is now down to nine months from the original 2-3 years through advances like computer-aided design and it is possible to configure a wide range of signal-conditioning functions on the same chip. With this in mind, conversion products will feature strongly in areas of advanced semicustom and linear i.cs.

## The next few years

Current technologies are capable of serving most of the identified needs. Immediate challenges are to continue to increase the number of functions offered in an i.c. to suit the endless number of analogue signal configurations.

Such products as gain-ranging, differential-input and multiplexed a-to-d converters, perhaps with on-chip sample-and-hold amplifiers, and all capable of 12-16bit operation are already scheduled.

Complete monolithic data-acquisition systems are now a reality. Multiple functions such as quad d-to-a converters and combined d-to-a and a-to-d conversion will continue to evolve and p.c.b. area will be reduced by a factor of five to eight through the application of small-outline packages. Faster single-supply devices will be possible when fabrication geometry allows 1.5µm widths.

However the need for even wider bandwidth product will be met by the development of bipolar-flash and GaAs technologies which by the end of the decade will be providing products to once again generate a whole new sales area.

*Information on specific conversion devices will appear in next month's issue*

# A mathematical rake's progress

by Ivor Catt

## Ivor Catt looks back on how he nearly became a maths addict

In my article of last November, I showed that Maxwell's Equations, so long thought to contain the heart and essence of electro magnetism, told us virtually nothing about the subject. Then, in my December article, I discussed the academic mafia's vested interest in knowledge (see panel). Here I try to discover who this group of charlatans*, the maths pushers, are. How does a young student grow up to become part of the social group who live by mathematical nonsense like Maxwell's Equations, and who conspire to prevent the development of a scientific subject in a proper, physical way?

Concern about this question led me to look back on my own education. What pressures were exerted on me to become a mathematical rake?

My experience indicates that the slide is similar to that of the drug addict — a number of small, apparently innocuous, slips downward, culminating in total separation from reality. As we progress through school and college, we are fed a series of potions, each more heady than the last.

The process started with the calculus. My introduction to it, at the age of 15, was worrying and disorienting. It was part of the great disaster which I thought had overtaken me in my first few months in the sixth form. Whereas I had always been good at maths, I found the first few months in the sixth form confusing. Even though Sam Richardson was a very good teacher, and I had help from my mother, a brilliant mathematician, at home, I couldn't understand the basis of what we were learning in mathematics, particularly the calculus.

This was a new experience for me. Previously, I had always found maths easy, and scored high marks. Now, suddenly, it was different. This was serious because if I tried to retreat from maths into some other field, all nearby subjects were based on maths anyway. There seemed to be no escape from my new-found inadequacy in mathematics. As the first half-year exams approached I became more and more worried, because still I couldn't grasp the basis of what I was being taught.

The flaw in the calculus package is what I now recognise as the reductionist fallacy a misconception which underlies and undermines western philosophy.* The error is to think that 'the whole is the sum of the parts', no more; that lots of bits of string are quite as useful as (and the same thing as) a long piece of string. Putting it another way, the problem of discontinuities was ignored. I was right to worry.

A whole array of misleading, damaging concepts slipped in with i, or j as we electrical engineers call it. "Two for the price of one"; if $a+jb = c+jd$, then $a=c$ and $b=d$; so we can do two jobs at once. Pretty, but a delusion, similar to the illusion that we can drive better after drinking, and for the same reason — our vision is blurred.

Hot on the tail of j came that awful array of cons under the appropriate descriptor 'sine'. I shall not develop this theme fully, but only repeat that one FRS went so far as to say that "Physical reality is composed of sine waves". In fact, the sinusoidal wave, which is a camouflaged circle, is Ptolemy's pure, circular epicycles fighting back against Kepler's less pure, more real, ellipse. Kepler, who himself loved the idea of the 'harmony of the spheres', saw a more pure 'equal areas in equal time' rather than a distinctly un-heavenly, earthy,

> ***"How does a young student grow up to become part of the social group who live by mathematical nonsense like Maxwell's Equations, and who conspire to prevent development of a scientific subject in a proper way?"***

*The Shorter Oxford English Dictionary entry for this word is particularly apt:

> **Charlatan** 1. A mountebank who descants volubly in the street; esp. an itinerant vendor of drugs, etc. . . .
> 2. An empiric who pretends to wonderful knowledge or secrets . . ., a quack.

However, if we then look up the entry for Empiric, the whole picture backfires on us.

*Titus, H.H., Living Issues in Philosophy. American Book Company, 1964, pp.148, 527, 540 etc.

### Mathematical mafia

The twisting of historical fact in the hands of the academic mafia is beautifully illustrated by the case of the discovery of the electromagentic theory of light. Obviously, a mathematician would like us to believe that the proposal that light was electromagnetic in nature resulted from subtle manipulations of his electromagentic equations by Professor Maxwell the mathematician. In fact, Whittaker[1] says that the proposal that light is electromagnetic came from Faraday in 1851, when Maxwell was 20. Now it might be asserted that the vague suggestion by Faraday was confirmed and strengthened by Maxwell's mathematics. However, Chalmers[2] says that there is an error in Maxwell's calculations, which "led Pierre Duhem to accuse Maxwell of adjusting his calculation so that he could arrive at a theory of light which he [or should we say Faraday?] already had in mind."

The truth appears to be that the idea preceded the maths; the maths was force-fitted onto the idea, like the ugly sister's shoe; and then the mafia claimed the maths generated the idea. The prince was not hoodwinked, and neither should we be. This racket, of forcing mathematical liturgy onto a reluctant discipline, constantly recurs in science, perhaps reaching its most grotesque in so-called 'computer science' courses.

1. E.T. Whittaker, A History of the Theories of Aether and Electricity, Nelson, 1951, p.194.
2. Chalmers, A.F., Maxwell and the displacement current, *Physics Education*, vol. 10, 1975, p.45.

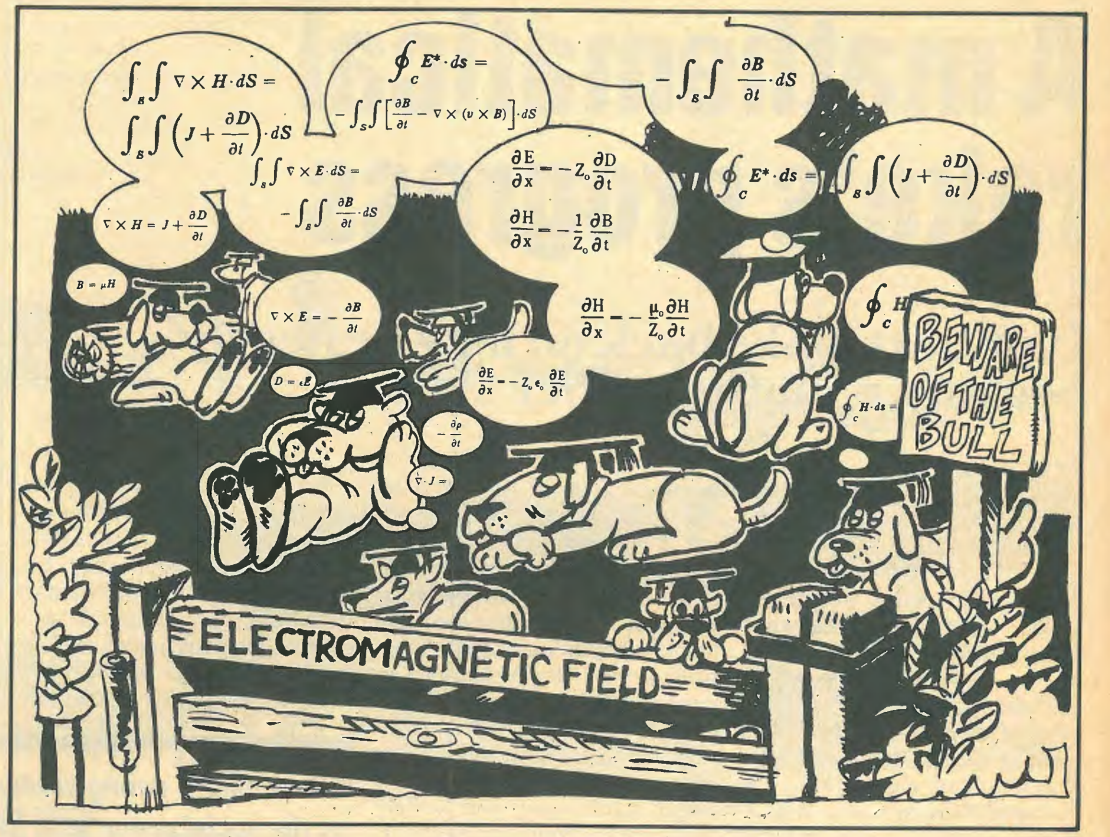
(we would say 'real',) ellipse.

The *Wireless World* July 1981 editorial, 'The decline of the philosophical spirit', contrasts the nineteenth century, when scientists were interested in and capable of distinguishing between the physically real and the mere mathematical construct, and today, when scientists no longer know or care about the difference, and have even developed a philosophy of science which confuses them.*

An example of the destructive effect of sine is the way in which it suddenly appears, unannounced and without justification, on the second page of a text book discussion of the t.em. wave.

In the event, my first half-year exams in the sixth form didn't seem too hard, and I felt that I must have scored over 50%, which would give me a breathing space in which to re-plan my future. To my astonishment, I learned that I had scored 99% and 92%.

However much I might *think* I didn't understand what was going on in maths, the marks I scored 'proved' otherwise. My high scores told me that I *was* still good at maths, as I had always been. However, a nagging suspicion remained with me that something was amiss. I doubted whether I could really have misjudged the situation so badly. Today, I believe that I was correctly judging the situation, and it was my exam marks that were wrong. I was being brainwashed into the belief that understanding was unnecessary, even impossible; that success meant the ability to manipulate the symbolism of the subject, not to understand it. I was being encouraged, the initial carrot being high exam marks, to turn the handle of the mathematical barrel organ, and not to ask too many awkward questions.




***"There is a similarity between the maths pushers and the drug pushers. Both entice the victim with promises of elysium. Both gradually increase the does. In both cases, there is nothing at the end of the rainbow."***

I seemed to learn my lesson, and later on, when taking A-levels, I gained a State Scholarship in maths although only 17 years old. This was a remarkable achievement, and should have secured my loyalty to the administrators of the mathematical myth. However, I was already questioning the usefulness of some of this maths, particularly the interminable geometry (since dropped) in the Cambridge Open exam, and so at Cambridge I decided to leave my strong subject, maths, and read engineering.* My background must have made me particularly sceptical. My mother had scooped the lot, gaining the top 'first' in maths in London University, but the payoff to her in benefits in later years proved minimal.

The next piece of blatant brainwashing occurred during my engineering course in Cambridge. We had a lot of thermodynamics, which was very mathematical. One day I asked my tutor, Professor Binnie, what practical interpretation I could place upon an equation containing a college of terms involving the three e's — energy, enthalpy and entropy. His answer was that I should not bother to look for a physical interpretation, but should merely regard it as a piece of algebra to be manipulated according to the rules of algebra. I was shocked by this, and I remain shocked today. Had I left maths and taken up engineering for nothing?

Whereas drawing, or draughting, was strong in the Cambridge Engineering Faculty and seemed to occupy a large part of our time, being the only subject you were not allowed to fail, electricity was weak, rating only one lecture a week, or at most two. One suspects that conservative Cambridge of the 1950s hoped that this new-fangled electricity thing would prove to be a flash in the pan, and go away soon. (Gaslight, I have been told, was very pleasant; much softer on the eye than electric light.) I suspect that my later success in elecromagnetic theory resulted from the lack of teaching in it that I had sustained while at college.

We did not cover the Laplace Transform, and this set me apart from upstart graduates from red-brick universities, who enjoyed discovering how backward Cambridge was. I was lucky in this omission, because I now feel that transforming is one of the destructive mathematical techniques in engineering that increases the divorce from reality, and which is the legacy to engineers from mathematicians. Whereas to me it is obvious from first principles that to get constant current through a capacitor* you need a continually increasing voltage, I recently found that for a student of Laplace this is the conclusion of a lengthy piece of complex calculation.

Thus was the stage set for Maxwell's Equations, that phoney apology for electromagnetic theory, which held sway for a century and so befogged the subject.

There is a similarity between the maths pushers and drug pushers. Both entice the victim with promises of Elysium. Both gradually increase the dose. In both cases, there is nothing at the end of the rainbow.

*Popper, K. Conjectures and Refutations, R.K.P., 1963, p.100

*I love the Heaviside remark; "Whether good mathematicians, when they die, go to Cambridge, I do not know." — Heaviside, O., Electromagnetic Theory, Vol. 3, Dover, 1950. (First published 1903.)

* using theory N





## 8085 single stepping

I stopped using d-type bistable i.cs in single-step circuits because of their erratic behaviour and the problems that they give with circuit layout. This reliable 8085 single-step circuit uses very few components, yet includes a logic probe which can fast transients. The probe runs from the step-circuit supply to avoid tangled wires.

It should be possible to use the unit to step 6800-series processors by connecting the ready-out signal to the 6800 halt pin and ALE-in to the VMA line. It might also work with 6502 processors with ALE connected to the SYNC pin and ready-out to the 6502 ready line. By injecting a negative pulse at the capacitor, slower automatic test equipment could be stepped. I have not tried these possibilities.

The probe's only disadvantage is that it cannot indicate a floating line. Using mos i.cs will make the unit suitable for other logic levels, but protection in the form of zener diodes will be needed.

Debouncing is carried out by the first latch. Output of this latch feeds a capacitor and pull-up resistor to give negative pulses. Normally, this method is avoided because of noise on the capacitor output, but in this case the latch triggers on a negative input. Once the latch is set, the capacitor charges and the 8085 runs until its ALE signal resets the latch. When this happens, the ready output halts the 8085.

R. Brain
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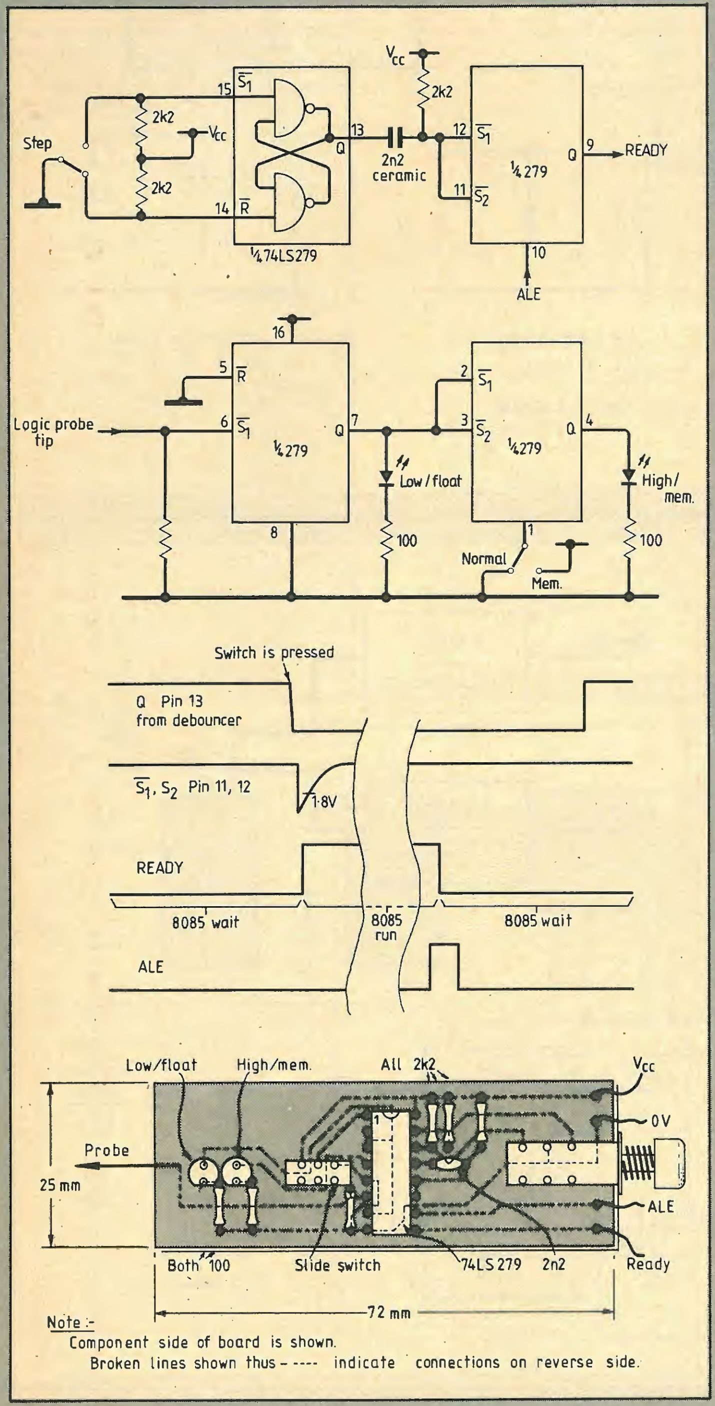



**DON'T WASTE GOOD IDEAS We prefer circuit ideas with neat drawings and widely spaced typescripts, but we would rather have scribbles on "the back of an envelope" than let good ideas be wasted. Submissions are judged on originality or usefulness — not excluding imaginative modifications to existing circuits — so these points should be brought to the fore, preferably in the first sentence.**

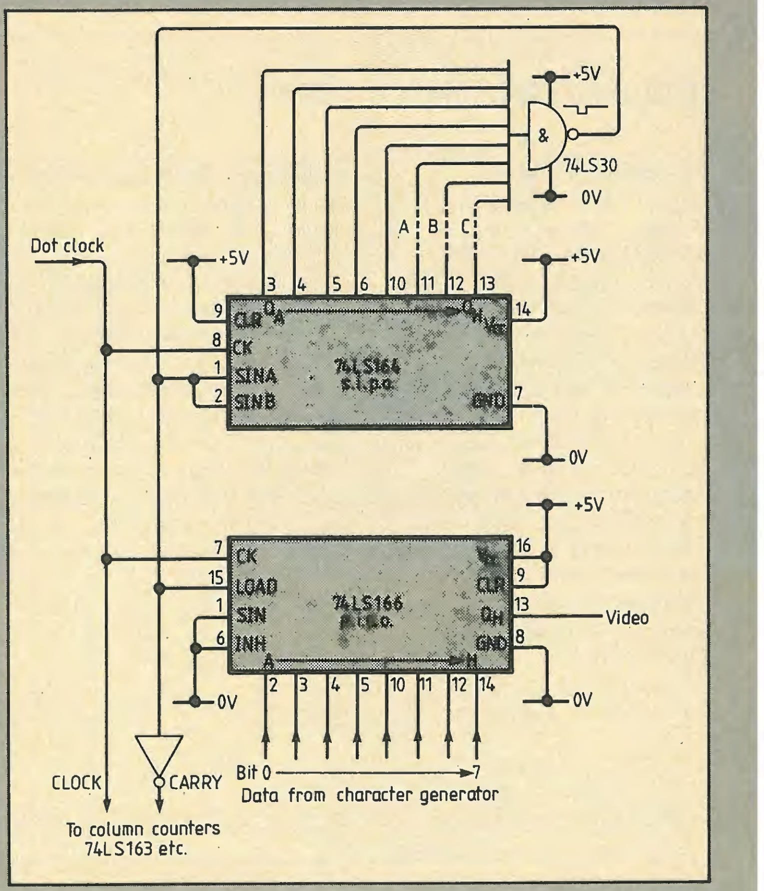
## Character generator dot clocking

Because of the speed of c.r.t. dot clocks it is easy to run into problems if synchronous logic is not used, especially around the parallel-in/serial-out device at load time. Strobe signals for data latches in the pipeline are often needed; delays in counters can drastically reduce the amount of time allowed for these and memory accesses.

This circuit, based on a recurring 'walking zero' principle, uses few i.cs to produce a serial-in/parallel-out shift register circuit providing up to nine consecutive strobe signals. For a six-dot font, links A, B and C are not used. Link A is used for seven dots, links A and B for eight dots and links A, B and C for nine dots.

A character clock for c.r.t. controllers or microprocessors can be produced by connecting the set and reset inputs of a bistable multivibrator to appropriate outputs of the serial-in/parallel-out circuit.

J.R. Charlesworth
Pickering
North Yorkshire



## Enhancing analogue meters

Measuring instruments with pointers are still preferred for many tasks but they are normally only useful for a minimum indication of 1% whereas 0.1% is often desirable. Logarithmic scaling gets round this problem.

A single diode can be used as a logarithmic converter but silicon diodes give a six-decade law, i.e. 1% of full scale corresponds to $10^{-6}$ of the input required for full scale. Germanium diodes do not generally follow the logarithmic law closely, especially at higher currents.

A diode-resistor network can give the required law and if several diodes are used, variations due to diode characteristics can be minimized. Using the diode network as feedback around a single op-amp as shown in the second diagram gives current output which is accurately proportional to input voltage.

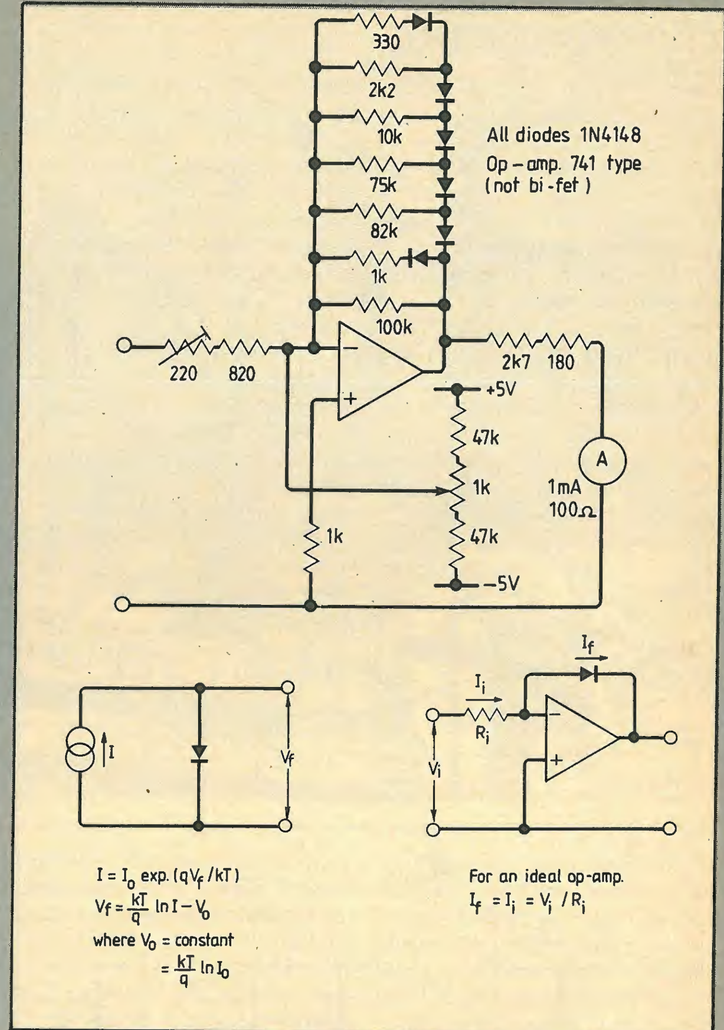
The final circuit uses five cheap unselected diodes in the logarithmic network and one to protect the meter against reverse-polarity input. Low closed-loop gain at high input voltages means that the input signal must be applied to the op-amp inverting input.

Up to the point at which the first diode conducts, in this case 10% f.s., the law is linear. Results are

| Input (mV) | Deflection (%) |
|---|---|
| 0.3 | 1 |
| 1 | 3 |
| 3 | 10 |
| 10 | 20 |
| 30 | 40 |
| 100 | 60 |
| 300 | 80 |
| 1000 | 100 |

Accuracy depends on temperature; if temperature compensation is needed a more complicated circuit using 'catching' diodes referenced to temperature compensated voltages may be used. This circuit was designed for the current meter of a bench power supply. Range switching is not necessary yet current drawn by low-power circuits is easily monitored.

J.M. Woodgate
J.M. Woodgate and Associates
Rayleigh



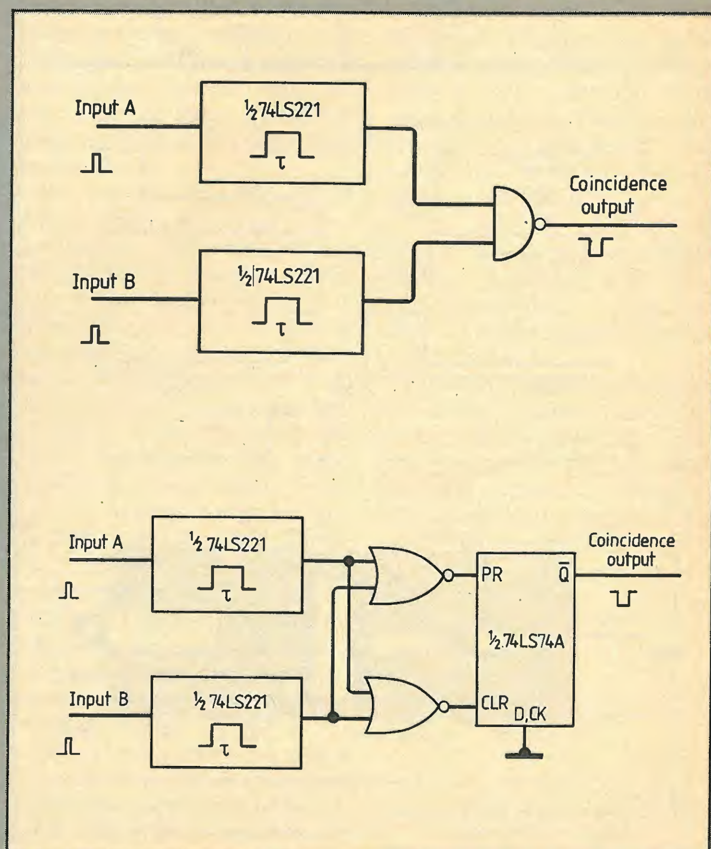

## Improved coincidence circuit

The common way of registering a coincidence between two input pulses within a resolving time $\tau$ is shown in the top diagram. It has the disadvantage that output pulses vary in width, being the duration of the overlap between the two input monostable devices.

If this output is used to drive t.t.l. circuits, erratic operation may occur as the result of the presence of pulses shorter than the specified minimum trigger duration. In particular 74LS123 and 74LS221 monostable i.c.s, when driven with pulses shorter than 40ns do not trigger but propagate a sharp glitch through to their outputs.

An improved coincidence circuit is shown below. The output pulse is of constant duration, $\tau$, the resolving time. If the overlap between the two input monostables is less than 25ns the 74LS74A bistable device will fail to trigger and no output pulse occurs. This, however, happens in a controlled manner with no output glitching.

John McMillan
Dept. of Physics
University of Leeds.




## Comparator for capacitor sorting

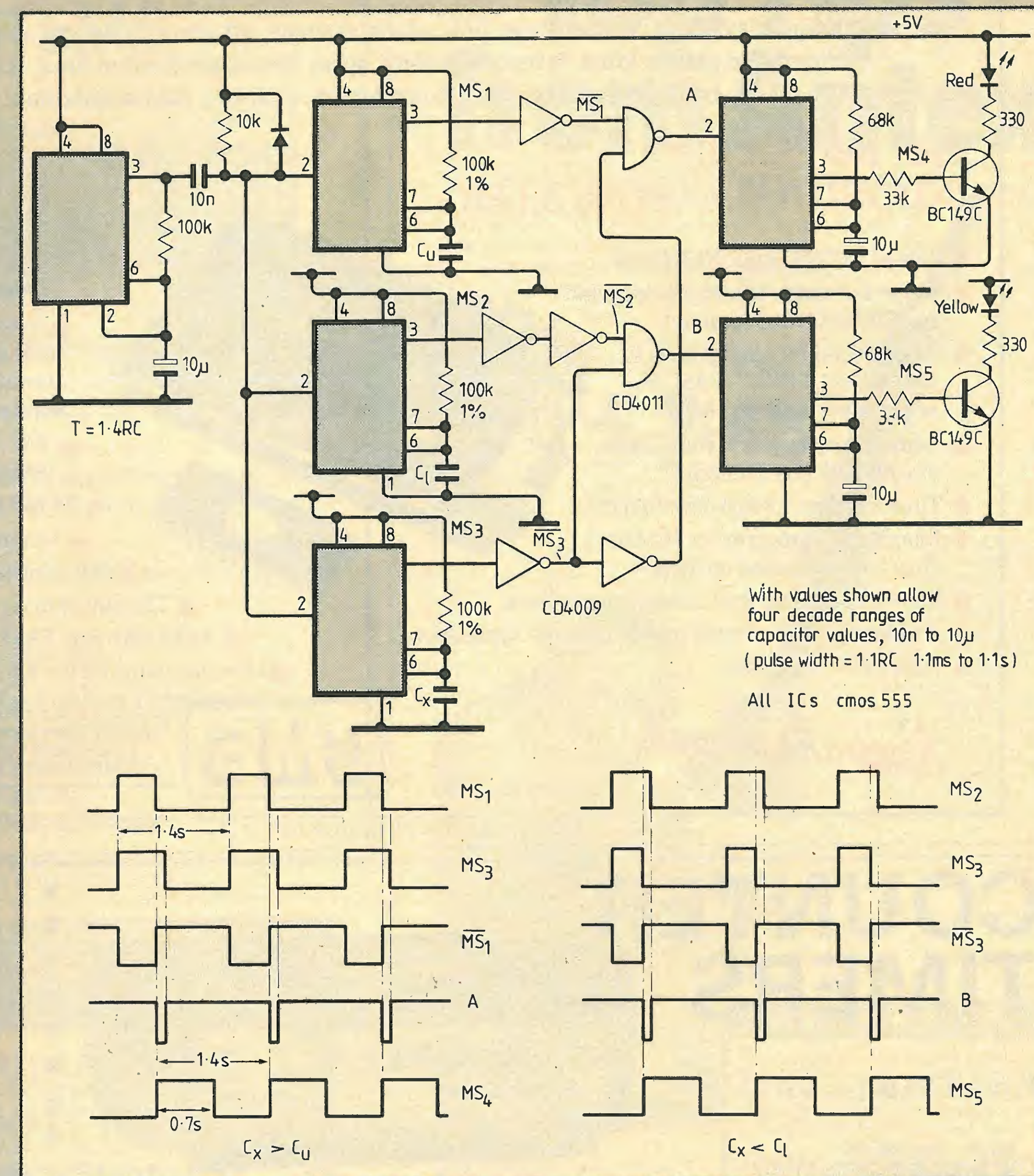
Conventional methods for sorting capacitors use either analogue or digital comparison techniques. This method compares the pulse width proportional to unknown capacitor $C_x$ with that of two known limit-value capacitances.

An astable multivibrator with 50% duty cycle and 1.4s period triggers three monostable elements representing upper and lower capacitance values $C_u$ and $C_l$ and unknown capacitor $C_x$.

When pulse $MS_3$ exceeds $MS_1$, the upper monostable i.c. is triggered and its led blinks at round 0.7Hz. When $MS_3$ is less than $MS_2$ similar gating triggers blinking of the yellow led. When neither led blinks, $C_x$ is within limit values set by $C_u$ and $C_l$.

Gate delays are adjusted so that false triggering of the output monostable i.cs does not occur.

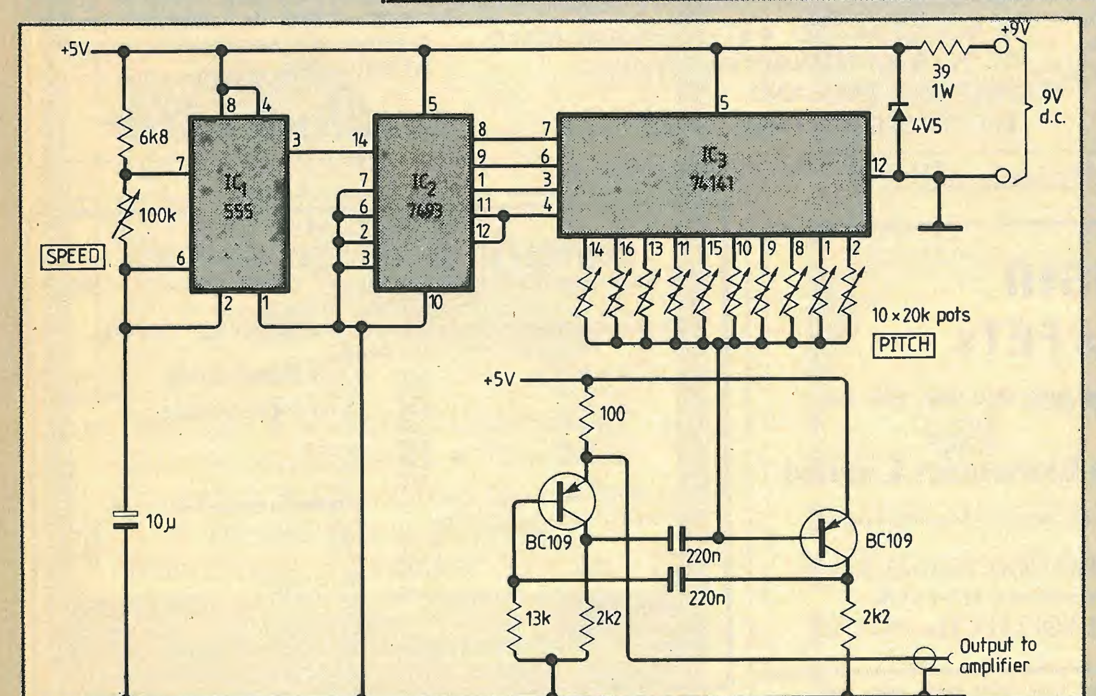
V. B. Kuber
Nashik Road
India




## Simple tunes

Speed and pitch are variable on this simple tune generator. The 555 clock drives a binary counter, output of which is decoded. For each step of the clock, potentiometers set pitch by determining frequency of the astable multivibrator.*

M.H.S. Bukhari
Hyderabad
Pakistan




**Diodes in output lines of the 74141 might stop interaction of the potentiometers. — Ed.*

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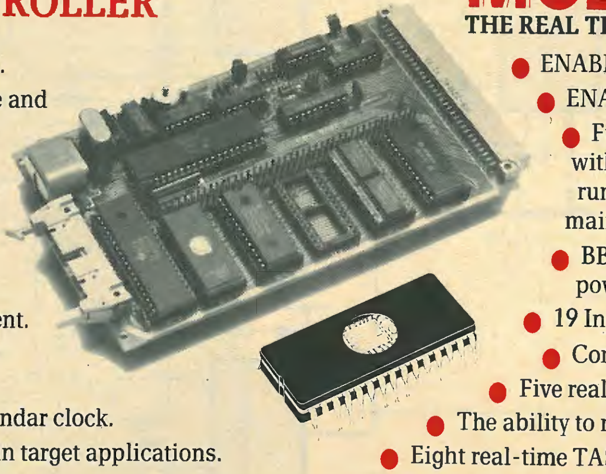

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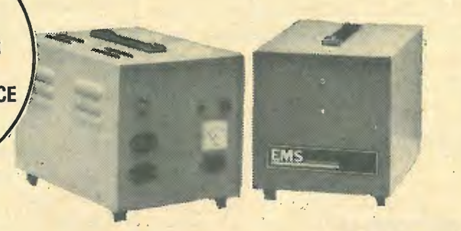

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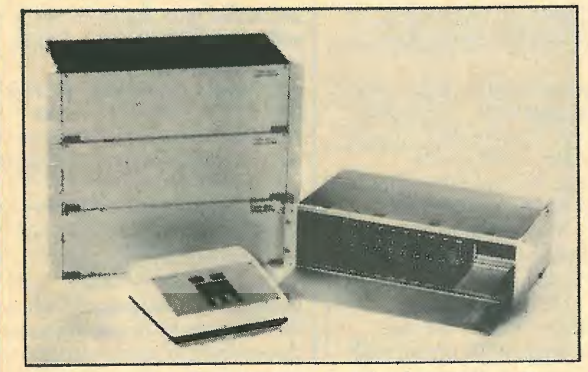

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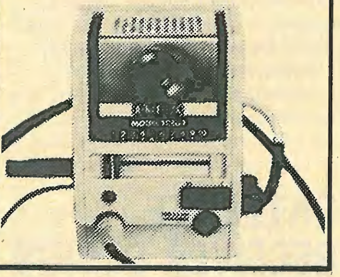

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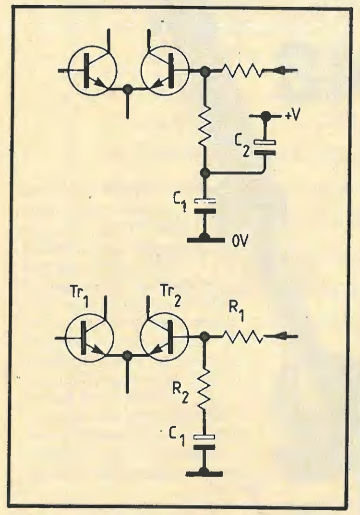
## ELECTROLYTIC CAPACITORS IN LONG–TAILED PAIRS

In audio terms, the main shortcoming of electrolytic capacitors is their behaviour when connected to the base inputs of long-tailed pairs, Fig. 1.




When leakage is present in $C_1$ a d.c. voltage divider is formed by $R_1$ and $R_2$ and is automatically taken into account when biasing the amplifier. When the leakage fluctuates however, as it will, biasing of the amplifier becomes unstable.

This instability can be eliminated by an additional capacitor, identical to $C_1$, inserted as in Fig. 2. By this means, leakage current of $C_1$ is supplied by $C_2$ instead of $R_1$ and $R_2$. It is asumed that a large value capacitor is connected close to the amplifier power supply input. If necessary, low frequency response should be curtailed prior to $Tr_1$.
H Wilkinson
Scarborough
North Yorks

## SATELLITE RECEIVER DESIGN

As a TVRO aerial engineer who is trying to add satellite tv systems to his range in order to make a living, I must raise a strong objection to the way you have allowed J.F.C. Hasting (Nov. 1985) to mislead your readers over the dish size required for domestic installations.

He might personally dream that 0.9 metres is the maximum diameter required, or he may glean it from old books (two years is very old in SATV), but experience anywhere in the UK is that 1.8 metres is needed from Intelsat V to give 99% merchantable quality, because 1.6 is giving 18 degraded days per year, approximately. 1.6 metres happens to be the largest diameter of dish that can be towed around in one piece without any difficulties whatsoever. The planners should take this into consideration.

I can only presume that Mr. Hastings was writing before UK DBS was aborted.
Peter R. Clark
Clark Aerials
Analby
Hull

## STEREO HISS

From Pat Hawker's report (*EWW*, September 1985, p.69) one can learn that efforts are being made to improve f.m. stereo transmissions. I refer to the discouraging s/n ratio often experienced in transmissions of the standard type.

In my opinion these efforts, which already have to face the uncomfortable facts of multi-path distortion, are based on a fallacy. The fallacy lies in the now out-moded concept that every improvement must be compatible with all previous systems and equipment in use.

With the present availability of cheap tuning equipment and components it is ethically possible to basically re-think stereo transmissions. Today the L + R signal takes up most of the power transmitted for reasons of compatibility to mono reception. However, mono reception and equipment are dead on the market place.

My conclusion is that there must now be a transfer to a new signal format tolerably acceptable to existing stereo demodulators only and which will deal with the two problems of s/n ratio and multi-path or phase distortion. This format could conceivably also finally solve the problem of television stereo sound.
Peter Hirschmann
Haifa
Israel

## NEW LOGIC SYMBOLS

At my school here, I offered a reward to anyone who could explain the working of the rom-selector (published in *WW* October 1983, p.59) straight from those gray boxes with 'phone numbers in them and spaghetti interconnecting them.

That offer has stood since 1983, and nobody has collected yet . . . Are continental students so dumb?

Mind you, this schematic is only a mild case.
J. Eyckmans
St. Truiden
Belgium

## ENERGY TRANSFER

I am of the opinion that Mr Parton (Feedback December 1984 and July 1985) has given the right twist to the electromagnetic arguments: metrology. I will disagree with Mr Parton's recommendation: to switch off mirth when switching on the Ampère.

I will disagree, too, with Mr Parton's criticism of the work done at the National Physical Lab. They tell us, I think, loud and clear: " . . . Not too seriously, chaps! Everything is wrong anyway. What does it really matter which false fact we begin with?" Right! Mr Parton may object to their objective assessment of the situation; apparently nothing seems to be the matter with the Ayrton-Jones gadget.

As recently as March 1985, *EWW* (p. 8, top of column 1) I reminded everyone once more that a neutron is as good a magnet as any super-conducting electric device, or even better. They lightly explain this away by the hope that inside the neutron (in its wave guise, I presume) electric charges are playing hide and seek at distances of $10^{-26}$m. An easy metrological problem, in other words. They can carry out measurements with an accuracy of 1 in $10^{30}$ parts, so no problem when defining the Ampère, we all presumed.

Mr Parton relies on rather old-fashioned standards. The latest craze in the Ampère field appears to be gadgets based on the magnetomechanical ratio of the proton (a thing they designate $\gamma_p$). And they threaten, with the help of this unlikely gamma, to reach, asymptotically, accuracies of (hold tight!) 1 in $10^{6}$ parts in the unforeseeable future. We may ignore, of course, the probability, but not likelihood, that they make a mistake and measure the gyromagnetic ratio of a neutron instead, which has an identical magnetic distribution, and then define the Ampère as the unit for strong currents of absolutely nothing.

So, I understood at last how it comes about that no circuit based on good design can ever work, except by chance, especially if using fancy components such as op-amps at 300 pA bias currents.

When we calculate such things on the drawing board, we have the certainty of at least 1in $10^{6}$ of calculating absolutely nothing.

Many more and even worse horror stories can be narrated by anyone going through metrology. I think *EWW* must take up the subject and give us information about this distressing situation.
G. Xenoulis
Toronto
Ontario
Canada

In a realistic physics all interaction should be treated as a discrete cause-effect process, which is intuitively self-evident from the principles of physical reasoning but it is not realised in present day theorising. Such a discrete process generates a power series as the interaction propagator passes to-and-fro and standard analytical techniques can be used to determine whether the series will converge to a finite limit or not. (The information accumulated in the series coefficients corresponds to the field exchange particles of high energy physics.)

If it tends to an asymptototic equilibrium the power series may be replaced by a more compact function from which the power series can be regenerated. The reversible correspondence between power series and generating function representing it is only valid within the radius of convergence for the iterative process of the cause-effect interaction.

This is the crucial problem for advance in theoretical physics: to develop a non-equilibrium behaviour with mathematically self-consistent formulae using continuous variables. Self consistency means that we *assume* that an equilibrium can exist between the variables (such as in a circuit) then proceed to calculate their would-be values.

For instance; Newtons laws of mechanics and gravitation and Einstein's relativistic modification of them, and de Broglie's 'wave' description for electrons in atoms, the formulae of electromagnetic theory and electronic circuit design. These all correspond to asymptotic equilibrium of a discrete interaction: the conditions of interaction under which these self consistent limiting descriptions are valid (as a calculation short-cut to a solution that exists is never even thought about.

The example I can quote is of feedback in a control system which I derived longhand in *WW* Dec. 1983. A finite time delay was supposed in a feedback control system and its response to the simplest possible stimulus of a unit step was described using discrete element analysis.

The 'operational amplifier' formula was rederived including valid limits for convergence, which is essential to understand the negative-feedback instability (so intuitively obvious) and why it is not predicted by the self-consistent op-amp formula. The self consistently derived op-amp formula is beautifully simple but wrong in principle, since the solution cannot exist (meaning well defined finitely stable behaviour) outside the region of convergence.

(As a matter of interest the Nyquist formula is just a special instance of the Curie-Weiss susceptibility law for a loose — coupled system and fits into a wider scheme of 'phase transition' formulae which includes the relativistic formulae for the limiting speed of light to material motion.)

Upon similar reasoning concerning what mathematical representations mean, the formulae of relativity and general relativity are calculation short-cuts. In all probability Einstein got the right answers for the wrong reasons. The de Broglie wave formula for equilibrium behaviour of electrons in atoms is a piece of brilliant insight but falls into the same classification of self consistency. A more fundamental mechanics is needed if we are to unify physics.

The Catt anomaly is based upon a misconception about the mathematical formulation of electromagentism; classical electromagnetism and its quantum, relativistic modifications can only be valid as a description for asymptotic equilibrium.

The response of any system (transmission line of interacting particles) to the transient of a step stimulus is a non-equilibrium phenomenon. hence the 'anomaly' vanishes as meaningless when it is recognised as an attempt to apply an equilibrium theory to a non-equilibrium situation. What is needed is a more general non-equilibrium theory from which to derive the equilibrium one as a special case.

E and M displacement current are not confused, as Mr Catt suggests (Letters, April). They refer to two separate aspects of an interaction, the asymptotic regime and the initial transient effects respectively where at the ultimate discrete scale of reality the mathematical sophistication of Fourier analysis is beautiful but useless.

Most worrying of all is the thought that the mathematical formulation of our physical laws (using continuous variables and compacted into generally applicable differential equations) implicity precludes certain phenomena from our reasoning which anyone with an ounce of physical insight would see as intuitively obvious though perhaps no so easy to quantify.

Algebra is just a noise-free information processing system (or medium) and logical manipulations do not add anything that is essentially 'new' beyond that physical insight which was encoded into the original formulation of the theory. As with any computing language if you put rubbish in you will get rubbish out; however, one needs to overcome the psychological barrier of the brazenly sophisticated formulae so spuriously created if we are to challenge the conclusions of the theory with *physical* reasoning to attempt unification.

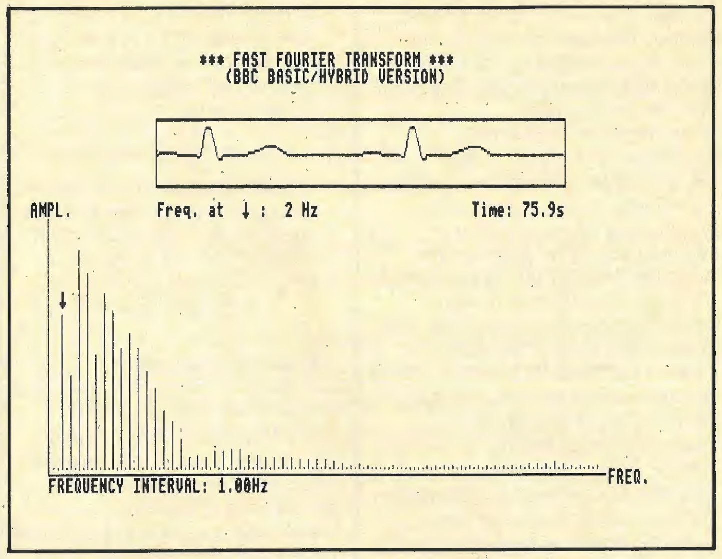
One needs to discuss mathematics in everyday language to truly understand what a formula (usually in a commutative or asymptotic cause-effect logic) represents and not to float adrift in a sea of assumedly understood.
P. J. Ratcliffe
Stevenage
Hertfordshire

## FFT

I have already spent several interesting hours with the Fourier transform program described by T. Larsen and G. Dyvik.

It is worth highlighting one very important rule which must be observed if correct transforms are to be obtained. The input data must represent an integral number of cycles, since the algorithm considers the data to be a repeating unit describing the waveform.

Measurements with a ruler on the heartbeat waveform show that the input data contains approximately 2.8 cycles of the basic waveform and hence the transform is of a very irregular heartbeat with every third beat shorter than the preceding two. Analysis of a similar set of data gave a transform close to that published.



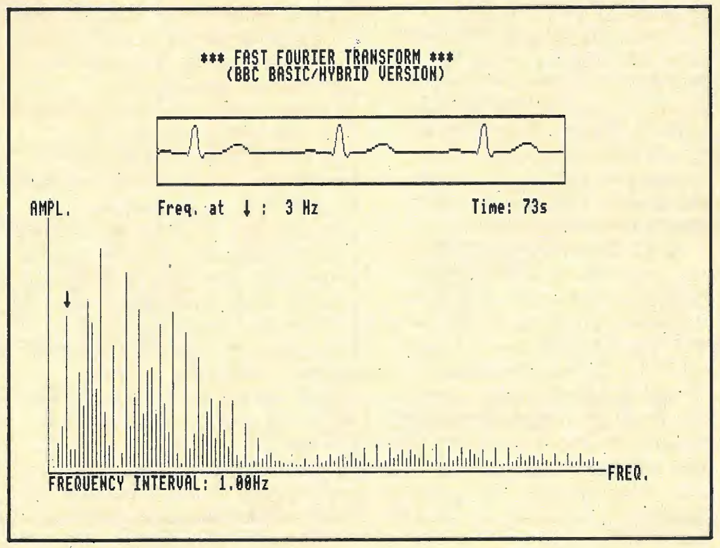

If exactly two cycles of this waveform are analysed then the true transform of a regular 'heartbeat' is obtained.

The analysis correctly shows a 2Hz fundamental and its harmonics.

The published program, almost unchanged, and with a printer routine was run on a standard BBC Model B microcomputer by loading the program from disc, moving it down in memory[1] and then inputting the data from tape. The time for the analysis is approximately doubled due to the increased data loading time but is still quite acceptable.
Peter H. Harris
Wimborne
Dorset

### Reference


1. Martin Phillips, *Acorn User*, August 1984, p.53.


## MOLECULAR ENGINEERING

Now everyone is familiar with what can be done with intregrated circuits and microprocessors, futurists and technophiles are looking to what will be the next wonder of science to hit the public imagination.

Various papers are now appearing in the United States that suggest one possible candidate is Molecular Engineering. This is the technology of "sub-millimeter machines, devices and replicating systems". Examples are Schneiker, C. Prospects and applications for genesis and ultra mass production of sub-millimeter machines, devices and replicating systems. (Cryonics, volume 6(5) May, 1983 p2•—30) and the book by Eric Drexler: Engines of Creation (Doubleday — to be published).

The possibility of such machines being self replicating means they will very cheap to produce, once they have been designed. The whole technology will be based on a bootstrap principle of building simple devices initially which will be used to make more complicated ones and so on. Whereas at the moment the public perception of such devices would be purely in medicine, in fact applications have been suggested in the computing and energy generation fields.

One often hears about the ability of biological molecular systems to record prodigious amounts of data. Although the speed of access may not be up to the best electronic systems, such systems could be used as a bulk storage device if a suitable interface could be designed. Furthermore, in the more distant future, it may be possible to engineer systems on a molecular level that are every bit as fast as present day electronic stores. Because they will be small and manufactured by the proposed submillimetre machines, they will be inherently cheap.

In the paper by Conrad Schneiker (which has a copious list of references), it is argued that the development of simple artificial replicating microtechnology devices should be possible this century. Most of the ideas used are not new, but draw from many different scientific disciplines. It is interesting to note that there wasn't anything by way of components in the Eniac computer of the later 1940s that wasn't previously available for 10 to 15 years. Again, the construction of the acoustic phonograph did not rely on any technologies that weren't available centuries earlier.

J. de Rivas
Truro
Cornwall

## WHAT'S IN A THEORY?

Our Ivor Catt always makes cheerful light reading, especially when he points out the obviousness of some physical statements which are usually mentioned only with bated breath. Typically, in *E & WW* for November 1985 he reminded us that only *uniquely electromagnetic* information contained in the two Maxwell equations relating $E$ and $H$ in vacuum lies in the theoretical artefacts $\mu_0$, $\varepsilon_0$; from them one can extrapolate to derive "the impedance of free space" as $Z_0 = \sqrt{\mu_0/\varepsilon_0}$ and "the universal velocity of light" as $C = 1/\sqrt{\mu_0\varepsilon_0}$.

The phenomenon is by no means confined to electromagnetic theory. Some of your readers might care to try the following unconventional derivation in the wave theory of matter:—

A completely general expression for 3-dimensional waves in any linear, continuous medium is provided by

$$\nabla^2\psi + \left(\frac{2\pi\varkappa}{u}\right)^2 .\psi = 0. \quad ...(1)$$

where $\psi$ (psi) is "whatever it is that oscillates" in the waves and $u,\varkappa$ are the wave velocity and frequency respectively. The last are classed as "unobservables" by the theory, so we will simply eliminate them by means of the wave axiom (self-evident truth) $u = \pi\upsilon$, obtaining

$$\nabla^2\psi + \left(\frac{2\pi}{\lambda}\right)^2 .\psi = 0. \quad ...(2)$$

Next, on the apparent evidence of experiment we assume these matter-waves obey the momentum precept $p = mv = h/\lambda$, so that

$$\nabla^2\psi + \left(\frac{2\pi}{h}\right)^2 p^2.\psi = 0. \quad ...(3)$$

Now the momentum $p = mv$ is directly related to the particle's kinetic energy $K = ½mv^2$ by the form $p^2 = 2mK$; substitution for $p^2$ leads inexorably to

$$\nabla^2\psi + \frac{8\pi^2 m}{h^2}K.\psi = 0. \quad ...(4)$$

Finally, since the total dynamic energy of any particle is defined as $W = (K + U)$, evidently $K = (W - U)$ and therefore

$$\nabla^2\psi + \frac{8\pi^2 m}{h^2}(W - U).\psi = 0. \quad ...(5)$$

Here we have derived Schrödinger's Wave Equation, that famous, basic statement of the Wave Mechanics which students may approach only with extremest reverence. Given two further assumptions it leads to Schrödinger's mathematical model of the atom — represented as an infinite set of spherical harmonics — which is said to "explain" the atomic line spectra.

The derivation given above may be unfamiliar, but it is both simple and watertight. Step by numbered step it consists of the following physical assumptions:—

(1) let us suppose that linear matter-waves exist;
(2) Then these matter-waves must obey the wave axiom;
(3) The matter-wavelength of a particle is related in this particular way to its mechanical momentum *(de Broglie)*;
(4) The laws of Newtonian mechanics are to apply; and,
(5) A particle's energy is part kinetic, part potential.

Given at (1) the idea of matter-waves and at (2) the axiom which must follow from that, the *only reference* made to any property of the waves, namely $p = h/\lambda$, occurs at (3). The derivation is in fact complete at this point, the other two steps being added to facilitate its practical application. We note that the derivation, and therefore the wave equation itself, is invariant with respect to any definition of $\upsilon$, so that "any old waves will do" for the wave theory of matter. That is why a Wave Mechanician will give you an odd look if you ask him about the *frequency* of his matter-waves. Nor is any textbook willing to tell us whether these matter-waves are transverse or longitudinal. The theory doesn't know about such things, and it gets away without caring about them either!

As Mr Catt has pointed out in the case of the electro-magnetic theory, so here in the case of the wave-mechanics, and so also as is well known in the case of special relativity, the key theoretical formulations are found to rest upon two, and only two, particular and radical physical assumptions. The rest is algebra.

W A Scott Murray
Kippford
Galloway

## HALL AND HOLES

To reply to R Petzeratt Nov.), the "standard explanation" of a "free seat moving backwards" is more realistic if one imagines a cinema (stalls, circle and balcony) rather than a doctor's waiting-room. The "hole" is now in a distinct minority; and I see a further analogy with the bubble in Bunker's Accelerometer — if the acceleration is to the right, the bubble moves to the right — to the great delight of teachers who are fed up with ticker tape timers — and everyone knows it is eally liquid which has moved to the left.

"Opposite" behaviour, depending on whether the charge carrier is in a minority or on roughly equal terms with the mob, also helps to explain the opposite effects of temperature on the resistivity of metals and of semiconductors. Consider a person trying to cross the town square, when it is densely packed. If the crowd is heated, it becomes more difficult to cross. But if the square contains just a few folk, and the charge carrier knows he (she?) must touch a different person (atom) before continuing, "heating" makes the journey easier.

May I suggest Dr J W Warren at Brunel University as being well qualified to say which of your many recent correspondents are blethering, and which are quite rightly attempting to pinpoint errors in existing theories? He has a long record of nailing fallacies perpetuated by text writers.

Bill Jarvis
MA, CPhys, MInstP

## Relativity

The idea that classical physics cannot account for the constancy of light velocity needs correction. The velocity will be constant if the fields of observers A and B, whose coordinates are related by the Galilean correspondence, both satisfy equations of Maxwell form. To express the fields of B in terms of those of A, let A change his variables tensorially with a Lorentz correspondence so chosen that his new equations are functionally identical to B's equations. The functions satisfying A's new equations and thus known, and B's fields are obtained by inserting his coordinates in the functions. The basis of relativists' beliefs is the Principle of Covariance which asserts that if any observer dares to change his variables then the resulting equations will be confiscated and given to another observer. Relativists should note how classical physics avoids their astonishing Principle but still gets their well-established formulae.

The difference between the two sets of fields at any point of 'absolute space' are the motional fields due to the relative motion of the observers. Conversely, such motional fields ensure the form invariance of Maxwell's equations and may be presented as the cause of the constancy of light velocity. A consequence is that relativists must seek justification outside the electromagnetic area since any valid relativistic calculation made in relation to an electromagnetic experiment can be described classically by using motional fields in lieu of 'motional space-times'. The falsity of claims that electromagnetic experiments disprove classical physics should be remembered when assessing the credibility of other claims that relativists will assuredly make.

1987 is the 300th anniversary of the publication of Principia and it would be nice to have the mess tidied up by then. The procedure is obvious — renounce the Principles of Covariance and thereafter respect the principles of mathematics. It will be found that all valid relativistic formulae will carry over into classical physics since the renunciation of the Principle of Covariance does not imply that tensor methods cannot be used.

R. Berriman
Palmerston North
New Zealand

## ENERGY TRANSFER

The reversed polarity of the Hall effect, referred to by R. Petzeratt in the November issue, is not confirmed to p-type semiconductors. The same phenomenon is found in certain metals, such as zinc and cadmium. The mater was a major anomaly until the late 1920s, when it was accounted for in quantum mechnics.

As regards Catt's views concerning electrical conductivity, he seems to have confused my reference (in the February issue) to electrons entering and leaving the conduction band (from and to the valence band) with the metal strips or "bands" ins triplines. This suggeests lack of appreciation of the physical realities, except for the out-dated "cannonball" electron from classical electromagnetism, that participate in the physical processeds in conduction, such as photons and psi waves. My main point was, and remains, that the velocity of electrons does not form a strong enough foundation from which to make such pronouncements as "the death of electric current" and "electric charge does not exist" (December 1980).

G Berzins
Camberley,
Surrey.

# Naiad training robot

## Third installment completes the description of the robot arm's various drives. Design by Dick Becker and John Wells

Axis 5, the gripper, also has a 16mm cylinder and this too uses a rubber seal, Fif. 16. Power may be either pneumatic or hydraulic. The two systems may be simply compared by minor re-plumbing. When operating hydraulically the whole system is self-contained. Pneumatic operation however is faster and the difficulties of servo-controlling a pneumatic system do not apply to a gripper, which requires only to be fully open or firmly clamped on-to the component being handled. There is a connector on the end panel of the robot which permits fitting to either an airline or to a cylinder of carbon dioxide when no airline is available. With a cylinder, as used for fizzy drink dispensers, there is sufficient capacity for over 1000 operations of the gripper. This cylinder together with its pressure regulator clips onto the side of the robot.

Both the hydraulics and the pneumatics of the Naiad are controlled by solenoid-operated valves in which there is a stainless steel plunger with rubber ends for closing off whichever orifice they are in contact with, Fig. 17. A spring normally holds the plunger in the down position and water can then flow from port 2 to port 3. When 24 volts is applied to the solenoid, the current causes magnetic flux to lift the ferromagnetic plunger, closing off port 3 and opening port 1. Each valve can thus be visualised as a 1 pole 2 way switch. Where only on-off valves are required in the hydraulic circuit, port 3 is omitted from the valve, Fig. 18.

Hydraulic power comes from a small vibrating-piston pump inside the robot base. It draws water from a bottle, acting as the sump, and pumps it into an accumulator. A hydraulic accumulator is a pressure reservoir and consists of a chamber into which the fluid is pumped, and a sprung wall that is displaced by the pressure. When demand exceeds the capacity of the pump, the wall returns providing additional fluid power. An accumulator may consist of a cylinder with a piston compressing the fluid, either by a helical spring or air pressure, but more frequently a rubber bladder or diaphragm with compressed air behind it is used.

Naiad uses a diaphragm-type accumulator consisting of a hemispherical dome with a sheet of rubber sandwiched between it and the top plate of the robot, Fig. 19. The cavity on the underside of the diaphgram is pumped up with air to 4 bar. Water is then pumped into the cavity between the diaphragm and the dome. The dome is made of cellulose acetate butyrate, which is transparent, and the action of the diaphragm rising and falling, depending on demand from the hydraulic cylinders, can be observed.

To have the robot under servo control, its position is sensed by a potentiometer fitted to each rotary joint. A stable 10 volt supply goes to each potentiometer, the wiper of which is connected to a high

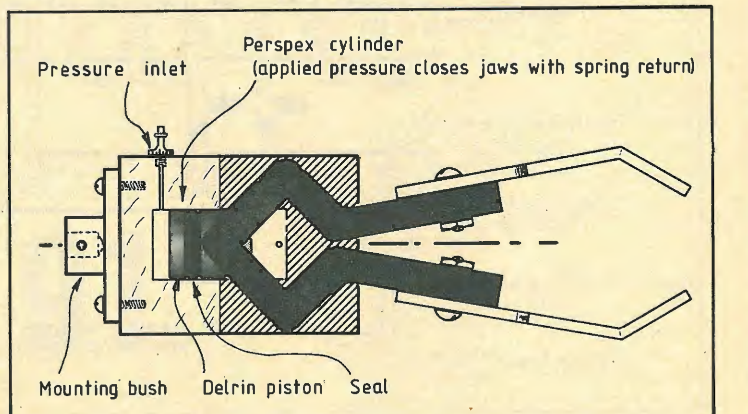



**Fig.16. Gripper is a Perspex cylindrical block with an axial cylinder. A spring retaining pin passes through the Perspex at the mounting bush end and a similar pin through a hole in the piston and through slots on opposite sides of the cylinder. Two longitudinal holes down the side of the cylinder act as spring guides and the springs are located on the pins. When air or water pressure is applied to the input port the piston is forced down the cylinder closing the jaws.**

### Naiad features

- Low-pressure hydraulics runs on water
- See-through Perspex cylinders
- DC servo and pneumatics included
- Built-in pump operates at 7 bar
- Built-in electronic control system
- Five servo-controlled axes + gripper
- Lifting capacity 500g
- Reach 500mm
- Parallel computer interface
- Software for BBC, C64, Apple IIe, IBM PC

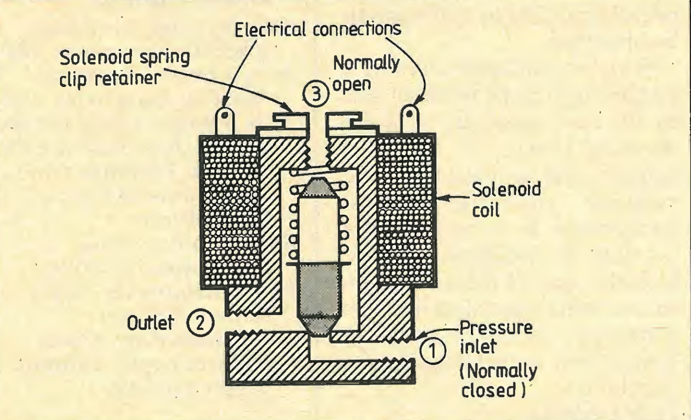
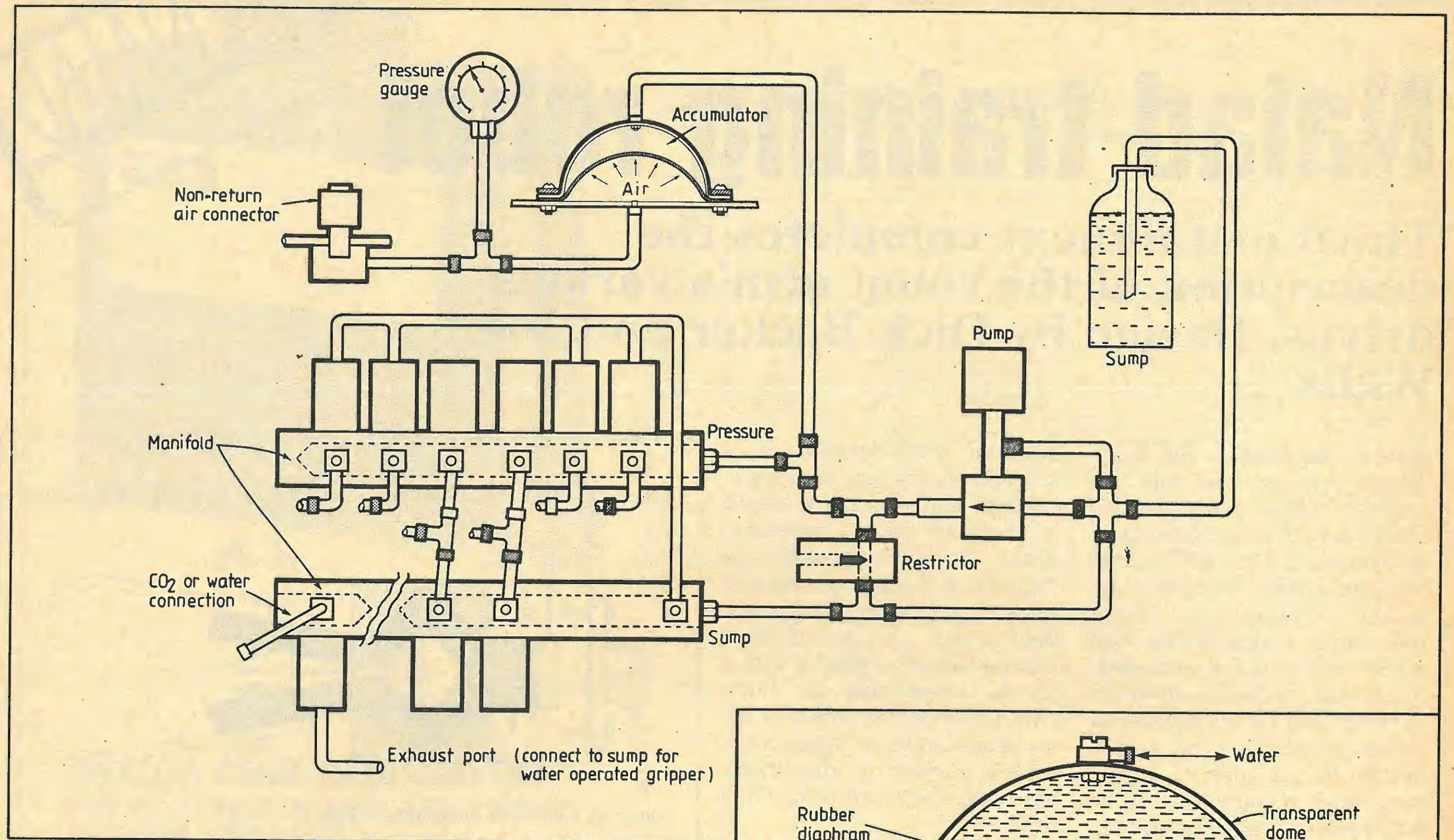



**Fig. 17. In the solenoid valve shown, valve is held onto its seating by spring pressure thus shutting of inlet port. In this condition there is free passage of fluid between ports 2 and 3. When a voltage is applied to the coil, plunger is pulled of the seating of the pressure port and seats into port 3. Flow is now directed from port 1 to port 2.**



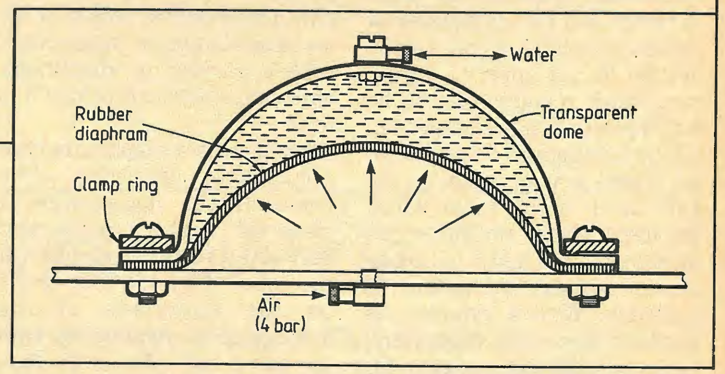




**Fig. 18. Hydraulic accumulator is first charged with air at 4 bar (60 psi) forcing diaphragm to take up the shape of the inside of the pressure dome. Water pressure is now applied to the connector in the top of the dome; when it reaches 4 bar, water begins to enter the chamber forcing the diaphragm down. As the diaphragm is forced down air pressure increases. No more water pressure is required to cause a further movement and so on. System stabilizes roughly in the position shown when the pressure in both parts will be about 7 bar. If a flow rate is demanded in excess of the pump capacity, extra flow demanded by the hydraulic system will come from the accumulator.**

impedance amplifier so that the voltage measured is linearly dependent upon the angular position of the axis. If linear potentiometers or l.v.d.ts had been fitted to the cylinders then there would be a complicated relationship between their output and the angle of the axis. Also with those methods the voltage-andle relationship is strongly dependent on offset errors, making computation of positions in world coordinates more difficult than it already is on a robot of this versatility.

Whilst the operation of a robot is much easier when there is a built-in servo system, Naiad uses software-servoing of the hydraulics to increase its versatility as an educational tool. With software servoing the solenoids are directly controlled by the computer in response to the instantaneously measured position, whereas with hardware servoing a robot requires only to have data defining its next position, and this is well illustrated by axis 3, which is the motor driven wrist elevation axis. The servo amplifier for this axis has software-selectable gain so the effect on accuracy and stability on underdamped and overdamped servo systems can be observed.

With the hardware servoing a single line in Basic sends an axis to its next position; software servoing Basic is not fast enough and a machine code routine running in the background is necessary. It's possible to use Basic to give tolerable results if only a single axis is being controlled and this provides another valuable comparison of techniques used in robotics.

*To be continued*

## Naiad specification

**Axis 0 (waist) Angular movement 180°. Axle centre 101mm above tp of base**
**Axis 1 (shoulder) Angular movement 90°. Arm length between axle centres 170mm**
**Axis 2 (elbow) Angular movement 90°. Arm length between axle centres 190mm**
**Axis 3 (wrist elevation) Angular movement 250°**
**Axis 4 (wrist rotation) Angular movement 320°**
**Axis 5 (griper) Jaw opening 60mm. Jaw pressure 20 newton. Distance from end of jaws and axis 3 axle 140mm**
**Repeatability 2mm**
**Lifting Capacity 500g**
**Reach (from axis 1 axle-centre) 500mm**
**Base dimensions width 380mm depth 220mm height 161mm**
**Control System Axes 0.4 under closed-loop servo-control**
**Position defined by 8 data bits giving angular resolution of 0.4%**
**Computer Interface: Parallel. Robot addressed as if part of computer memory. Connects to 1MHz bus of BBC, expansion port of C64, slot of Apple or IBM PC.**
**Software: Accepts commands in Basic or machine language.**
**Software provided: Extensive package of Basic programs including direct control from computer keyboard, control by simulator, sequence storing, replay, sequence editing, sequence storage on disc and graphical display of robot dynamics, on disc for BBC, C64, Apple IIe, IBM PC computers.**



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# Volume 91 1985

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## Author index



# Synchrodyne a.m. receiver

by J.L. Linsley Hood

## Synchronous demodulator design gives low distortion, variable selectivity and freedom from whistles

In the days when the description 'radio receiver' almost invariably meant a system for receiving amplitude-modulated signals, a large number of good quality a.m. sets were available. Their major limitations were mainly those imposed by external considerations, such as reception conditions or overcrowding of the broadcast bands.

However, with the widespread adoption of v.h.f./f.m. broadcasting a number of changes have occurred — not all of them of direct benefit to the user. Because of the very high signal quality obtainable from a well-designed f.m. receiver, a very great deal of development work has been done on such systems, largely as a result of the interest of the hi-fi fraternity, in exploiting the low distortion, low noise and wide bandwidth of the transmitted signal.

Sadly, all this useful and beneficial development work in the f.m. field has completely passed by the users of a.m. broadcasts on the long and medium wavebands, presumably because it is assumed that the quality of signal normally available on these bands is so poor that it does not warrant high quality in the equipment used to receive it.

This has led to the curious situation that the owner of good quality audio equipment is likely to have no facilities at all for a.m. reception; or if his f.m. receiver does contain an a.m. section, it is unlikely to be much better than that of a low cost transistor radio.

This would not matter much were it not for the relatively limited range of f.m. transmitters, which restricts the choice of programmes available to the listener, and for the fact that some broadcasters (including the BBC) choose to transmit significant parts of their programme output on a.m. only.

### Basic receiver requirements

Some worthwhile improvements to the conventional a.m. receiver would be

- a low distortion demodulator system
- the avoidance of whistles often found with superhet-type receivers as a result of the interaction of signal and local oscillator harmonics
- a fully-variable selectivity, to reject adjacent-channel signals
- a truly flat-topped bandpass curve.

Sensitivity and resistance to fading are also highly desirable but they are normally quite well met by existing superhet designs. Any alternative system should be at least as good in these respects.

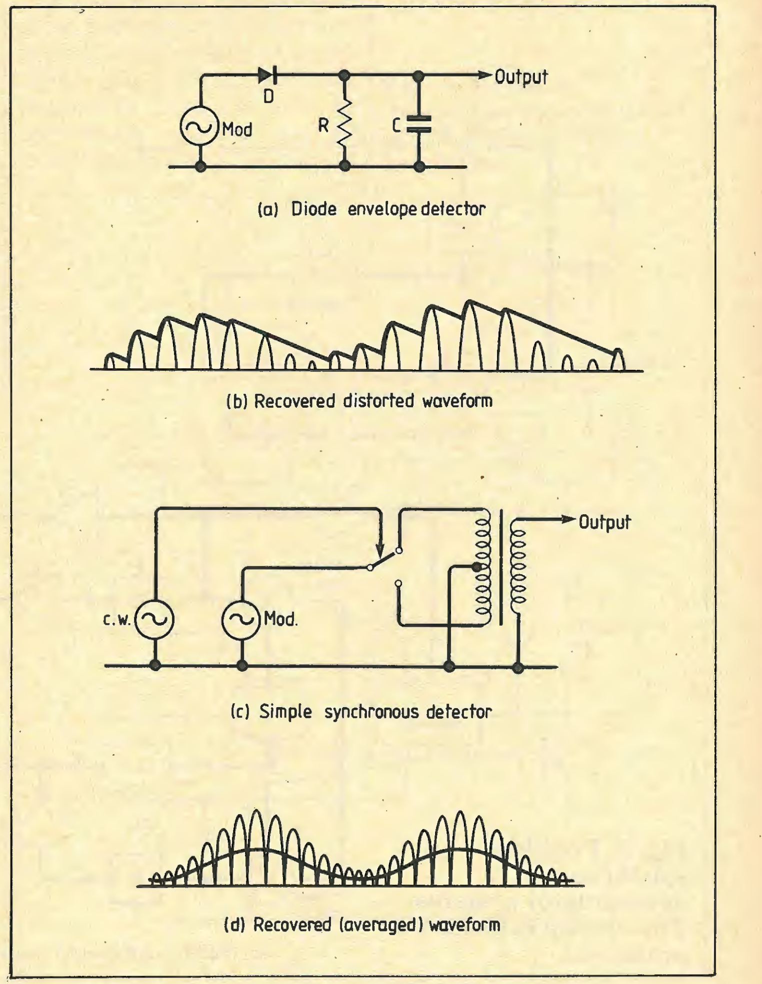
Given a good receiver system the signal quality available from many a.m. radio transmitters can be extremely good, and not a lot inferior to that from an f.m. receiver. This encourages the search for something better than the contemporary low cost transistor superhet.

An almost complete satisfaction of the requirements listed above is offered by a system based on a synchronous demodulator such as the synchrodyne or homodyne circuits, and the adoption of this type of approach has been strongly urged by Hawker[1], Herbert[2], Macario[3] and Padwick[4].

There is some ambiguity in the published literature in the use of these terms, so I propose to adopt the convention that *homodyne* refers to a system in which the incoming signal carrier, stripped of its modulation either by clipping or by side-band limitation, is used as the reference signal in the synchronous detector, and that *synchrodyne* refers to a system in which the reference oscillator signal is generated by a potentially free-running local oscillator.

In both of these systems, when the incoming signal is mixed in a multiplicative product detector or a phase-sensitive detector, the output will be a heterodyned signal

**Fig. 1. Diode envelope-detector (a), used in the majority of conventional a.m. radios. The recovered waveform (b) shows distortion. Below, a simple synchronous detector (c): the received modulation (d), recovered by averaging, is distorted much less.**



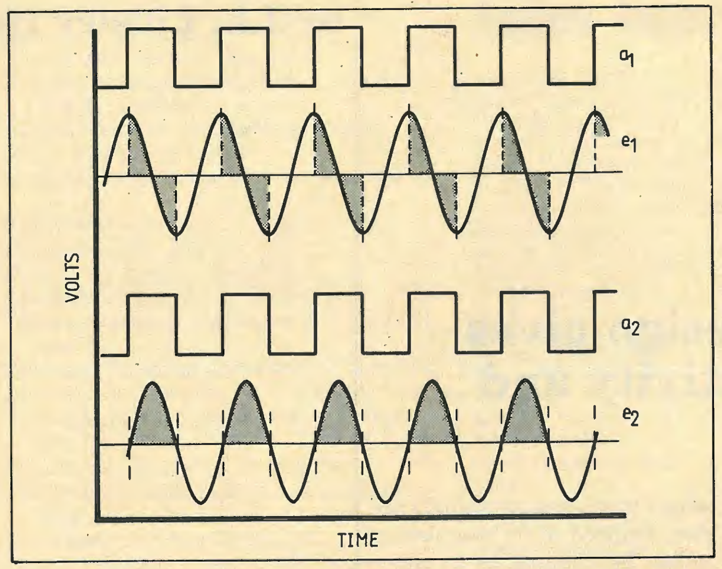



**Fig. 2. How the phase difference between oscillator ($a_1$ and $a_2$) and incoming carrier ($e_1$ and $e_2$) influences the output voltage (shaded) of the synchronous demodulator of Fig. 1(c). When the input waveforms are in quadrature (top), the net output is zero.**

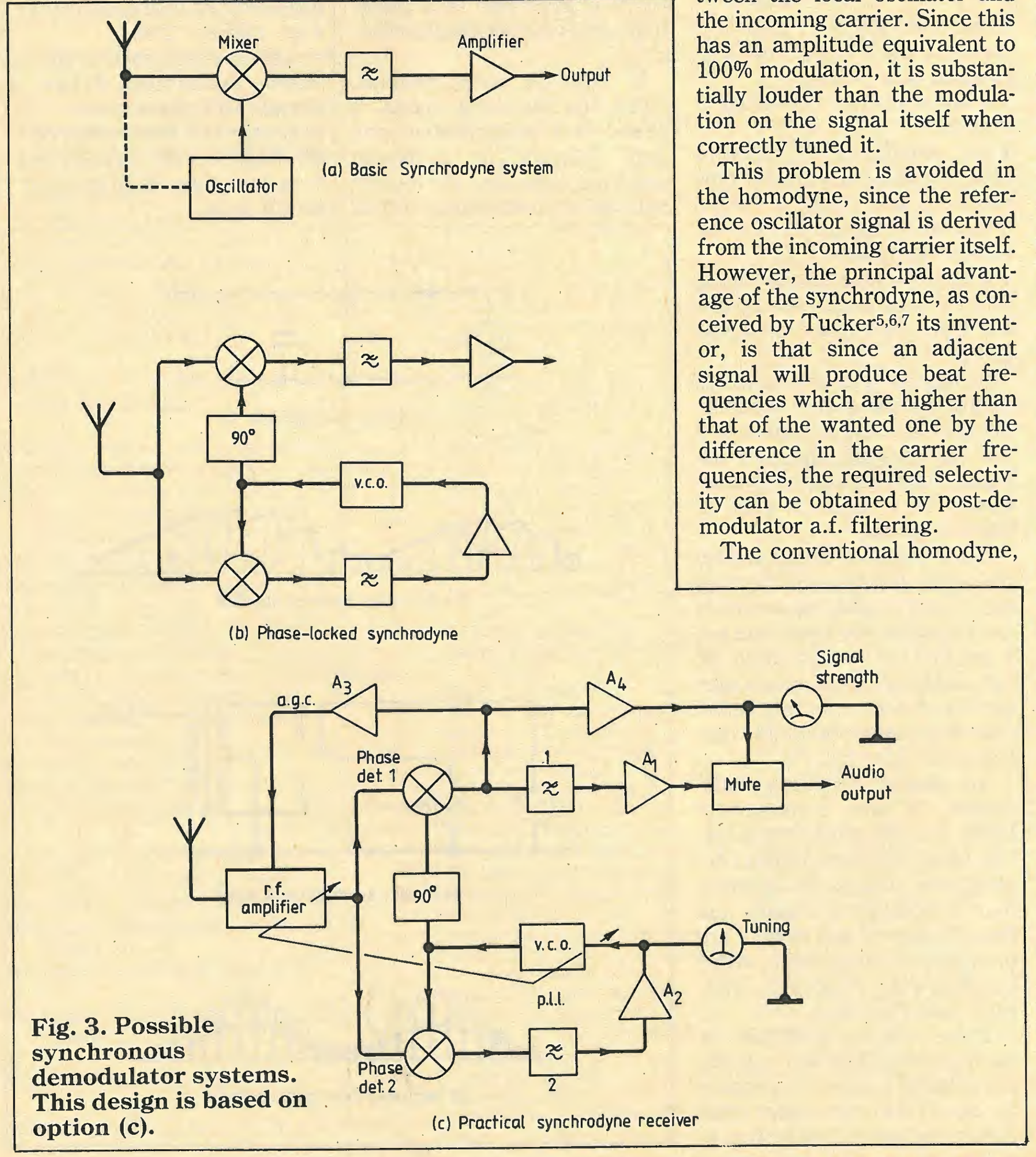



**Fig. 3. Possible synchronous demodulator systems. This design is based on option (c).**

having a zero beat frequency, leaving just the carrier modulation — the sidebands — as the residual signal. Since the process is simply one of transformation of the carrier frequency down to zero, the system is, in principle, quite linear and the harmonic distortion inherent in any rectifier-based envelope detector can be avoided. I have illustrated the comparative performance, in the case of a high modulation depth, in Fig. 1.

However, there are snags which are sufficiently daunting to prevent this otherwise excellent system from being widely adopted.

## Snags

In the case of the synchrodyne, the major problem is the piercing whistle which occurs as the station is tuned in, or detuned, because of the a.f. beat note between the local oscillator and the incoming carrier. Since this has an amplitude equivalent to 100% modulation, it is substantially louder than the modulation on the signal itself when correctly tuned it.

This problem is avoided in the homodyne, since the reference oscillator signal is derived from the incoming carrier itself. However, the principal advantage of the synchrodyne, as conceived by Tucker[5,6,7] its inventor, is that since an adjacent signal will produce beat frequencies which are higher than that of the wanted one by the difference in the carrier frequencies, the required selectivity can be obtained by post-demodulator a.f. filtering.

The conventional homodyne, in which the carrier of the incoming signal is demodulated simply by amplitude limiting, cannot offer this advantage of post-detector selectivity, since any incoming carrier will be treated equally. If pre-detector selectivity has not given adequate carrier discrimination, post-detector a.f. bandwidth curtailment cannot do so either.

If the circuit is a superhet, in which the i.f. frequency is fixed and predetermined, the required carrier isolation can be attained by a very narrow bandwidth circuit, such as a simple crystal filter. But this has the snag that small adjustments in tuning will lead to large changes in the relative phase of the recovered carrier, with consequent large changes in demodulator sensitivity.

This effect arises for the reasons which I have shown graphically in Fig. 2, with reference to the simple synchronous switch demodulator of Fig. 1c. If the relative phase of the incoming carrier and the switching waveform are at quadrature, the averaged d.c. output in any one limb of the demodulator (illustrated by the cross-hatched portion in the drawing) will be zero. Since this will be true for a carrier of any amplitude, provided that it is symmetrical, it follows that changes in the amplitude of the carrier (for example, produced by amplitude modulation) will have no effect on the output. Therefore the modulation will not be recovered.

For full recovery of the modulation envelope, it is essential that the switching waveform shall be accurately synchronized in phase with the incoming carrier. This is in addition to the requirement, for whistle avoidance, that it should be in frequency synchronism, which presents some difficulties.

In the case of single-side-band, suppressed carrier amateur radio reception, neither frequency nor phase synchronization are so critically important, and synchrodyne systems, with stable, free-running local oscillators have been more widely adopted. They are usually referred to as direct-conversion receivers.

## Synchrodyne receivers

The simplest functional synchrodyne system of the type proposed by Tucker[4] is as shown in Fig. 3a. In this, no specific aerial tuning is employed, and the signal which is selected is simply that which is in synchronism with the oscillator. Frequency and phase synchronism are achieved by injecting a small amount of the incoming aerial signal into the oscillator circuit, to induce it to pull into lock.

While such a system can work, especially when there is a strong local station, it is difficult to get the local oscillator frequency sufficiently stable.

A much better system is that shown in Fig. 3b, in which two mixers are employed: one to demodulate the incoming signal and one to operate a separate phase-locked loop system controlling the frequency and phase of the reference oscillator. This is a well-known technique, and practical examples have been described by Leopold[8] and Warsham[9].

Since the operation of the phase-locked loop (p.l.l.), for reasons which will be discussed later, is such as to force the controlled oscillator into synchronism at quadrature to the phase of the incoming carrier, a 90° phase-shift network or its equivalent must be interposed between the output of the local oscillator and the signal-demodulating mixer.

With some elaboration, this kind of system will form the basis for a practical synchrodyne receiver, which could be used domestically without any undue difficulty in operation. Such a system is shown in outline in Fig. 3c.

## A practical synchrodyne

As I have mentioned, there are a number of practical problems inherent in the synchrodyne system which must be remedied before such a receiver can be considered a usable alternative to the conventional superhet. Of these, the two most intractable (in the case of a simple direct-conversion system without pre-tuned r.f. stages) are those associated with the cross-modulation of the mixer system, and those associated with spurious signal reception due to oscillator harmonics or the inevitable non-linearities in the mixer.

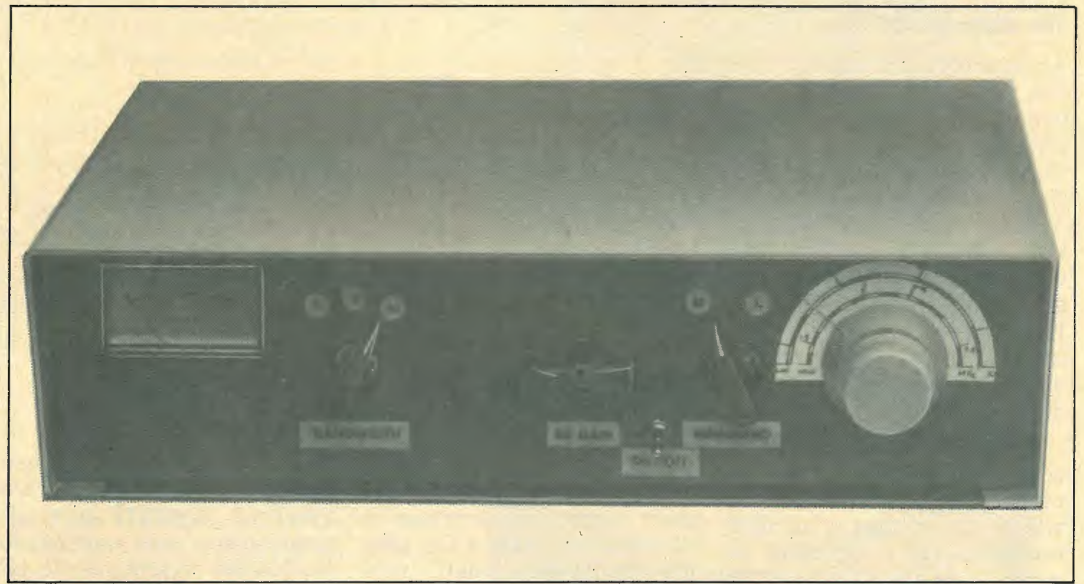
A pre-tuned r.f. stage is of great benefit in both of these cases. Firstly, it allows some form of automatic gain control, to prevent the signal level reaching the mixer from exceeding the level at which excessive cross-modulation occurs (typically in the range 30mV to several volts, depending on mixer type[10]). Secondly, it will provide enough selectivity to avoid spurious signals due to signal or oscillator harmonics.

Also, because some degree of r.f. gain reduces the need for high post-demodulator a.f. gain, the problems of aerial-sourced earth-loop mains hum and tuned-circuit microphony are greatly reduced.

Since the output of the signal demodulator will contain a d.c. component, this can, with suitable amplification, be used as a highly specific source of automatic gain control (a.g.c.) voltage, and also as a control voltage for a signal muting circuit to suppress a.f. output when the receiver is not on tune. This will remove the unpleasant whistle characteristic of a synchrodyne receiver when it approaches or leaves the point of synchronization with the incoming signal.

The practical benefits of such a receiver are considerable. They include, in addition to freedom from whistles and easy adjustment of the adjacent channel selectivity to suit listening conditions, a very low distortion demodulated a.f. signal and a very clean low-noise background. This arises because, in contrast to the diode envelope-demodulator which will demodulate any signal presented to it (including wide band noise), the synchronous detector will demodulate into the a.f. band only those signals which are within the chosen a.f. bandwidth of the synchronous oscillator frequency.

Also, the combination of a synchronous demodulator with an a.f. muting circuit gives a situation whereby when the receiver is tuned through the receiving band, there is complete silence between stations. The only signals received are those from perfectly tuned stations having a signal strength above some predetermined and presettable level. On first acquaintance, this is an interesting and novel experience.



**John Linsley Hood's phase-locked synchrodyne a.m. receiver covers both long and medium wave bands, giving low distortion, low noise, adjustable selectivity and whistle-free tuning. A kit of parts will be available from Hart Electronics.**

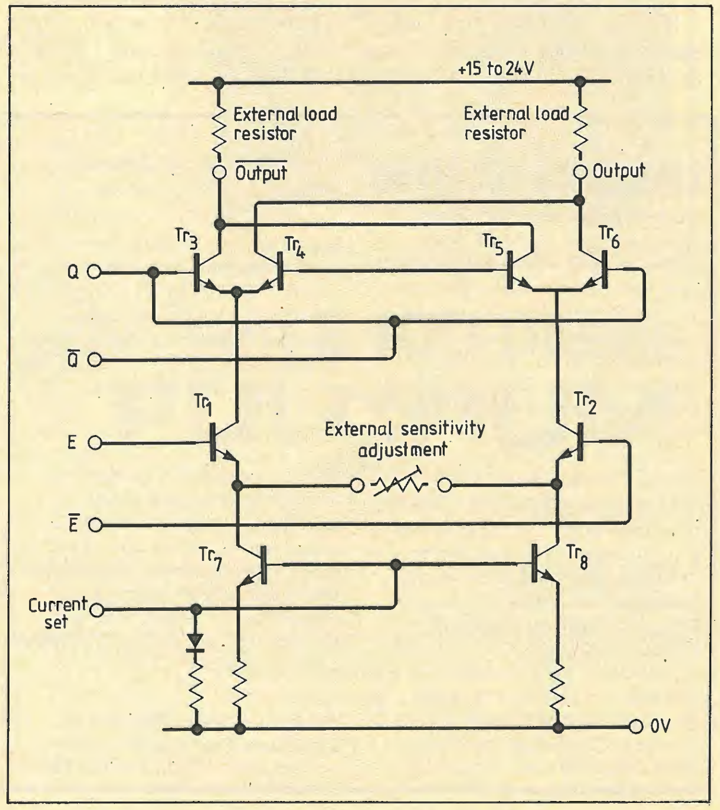



**Fig. 4. Balanced modulator-demodulator of the 1496-1596 i.c. family.**

### The phase-locked loop

There are certain types of circuit arrangement in which the output depends on the relative phase of two inputs. The synchronous switch of Fig. 1c is a simple and primitive example. A rather more elegant one is the balanced modulator demodulator arrangement shown in Fig. 4, using the LM/MC 1496/1596 family of integrated circuits. These can be described as phase-sensitive detectors (p.s.d.).

If such a p.s.d. is used as a comparator element in the circuit layout shown in Fig. 5, where a voltage-controlled oscillator (v.c.) is used to generate the second input ($f_2$) to the p.s.d., then the output of the p.s.d. will be a complex waveform ($f_1 \pm f_2$), containing the sum and difference frequencies of the input signal ($f_1$) and the signal from the v.c.o. ($f_2$). The output from the low-pass filter will contain simply the difference frequency ($f_1 - f_2$). If the difference in frequency between the two signals is very small, the output will be seen to vary from a positive potential, through zero, to a negative potential, and back again, as the instantaneous value of the relative phase of the two signals moves from in-phase, through quadrature, to out-of-phase, and so on.

If this difference frequency signal is suitably amplified and applied as a control voltage to the v.c.o., the operating frequency of the v.c.o. will alternately increase and decrease to a point at which the v.c.o. falls into appropriate phase synchronism with the incoming signal.

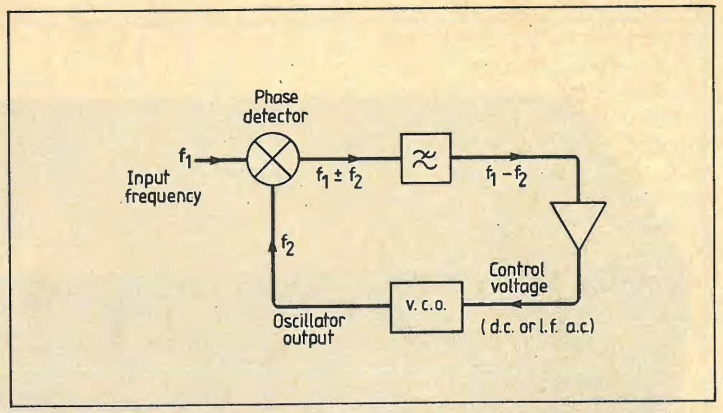


**Fig. 5. basic phase-locked loop arrangement.**

Further, if the free-running frequency of the v.c.o. is adjusted so that it coincides with the input signal frequency, with zero control voltage, then when the v.c.o. falls into synchronism (i.e., when the loop is locked) the required output from the p.s.d. and filter will be zero volts. This condition is met only when the phases of $f_1$ and $f_2$ are at quadrature. If the gain of the loop amplifier is high enough, the phase-quadrature condition is met even if the actual, and free-running frequencies of the v.c.o. are somewhat different.

A theoretical condition (I say this because, in practice, minor circuit malfunctions prevent this ideal circumstance from being fully realised) is that, when the loop is locked and the two applied signals are at quadrature, any amplitude modulation present on the incoming signal will be suppressed. In reality there will always be a residue of a.m. present on the p.s.d. output, which can introduce an undesirable measure of frequency (or more strictly, phase) modulation of the output of the v.c.o.

Two approaches can be employed to minimise this snag: to use the lowest amplifier gain practicable; and to make the pass band of the low pass filter as narrow as possible.

Both have the snag that they limit the capture range of the loop. Ideally, the loop should be able to jump into synchronism from a difference frequency which is moderately large, otherwise it will be difficult to capture the required signal when tuning through the waveband. Inevitably, some compromise is required on this point.

The reason why phase modulation in the v.c.o. is so undesirable is that it introduces a measure of second-harmonic distortion into the audio output of the demodulator p.s.d. (Phase det. 1 in Fig. 3c), thereby diminishing the practical advantage in linearity which such a system offers in comparison with the simple envelope detector.

It is nevertheless possible to achieve a reasonably satisfactory compromise, and in the following part of this article I shall describe an l.f./m.f. a.m. receiver employing the type of circuit design shown in Fig. 3c. This gives a sound quality noticeably better than that of the conventional type of a.m. receiver.

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2. Herbert, J.W., *Wireless World*, September 1973, 416-419.
3. Macario, R.C.V., *Wireless World*, April 1968, 52-57.
4. Padwick, G.C., *Electronics and Power*, March 1967.
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6. Tucker, D.G., *Electronic Engineering*, September 1947, p.276.
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9. Warsham, G., *Wireless World*, August 1972, 358-363.
10. Bryant, J.M., Radio Communications Handbook (Plessey Ltd), 59-60.


## Literature received

**Product guide from Dataman** describes their Gang-of-Eight eprom programmer, the Superdoc automatic test module for microprocessor-based systems and a wide range of other 'micro engineering tools'. Dataman, Lombard House, Cornwall Road, Dorchester DT1 1RX. **EWW 250** on the reply card.

Gothic Crellon have published a 500-page **buying and engineering reference guide** which lists, and also provides data on a wide range of semiconductor devices including the products of Motorola, Mullard, National, Plessey, RCA and Rifa. Connectors, switches and passive components are also included. **Gothic Crellon**, 3 The Business Centre, Molly Millars Lane, Wokingham, Berks RG11 2EY. **EWW 251** on the reply card.

Switched mode, linear and hybrid **power supplies** along with d.c./d.c. converters are listed in a shortform catalogue from **Coutant Electronics Ltd**, Kingsley Avenue, Ilfracombe, Devon EX34 8ES. **EWW 252** on the reply card.

B&R specialize in Connectors, fuses and circuit breakers, switches, indicators, meters, relays and resistors and detail them in a **components catalogue**. **B&R Electrical Products Ltd**, South Road, Temple Fields, Harlow, Essex CM20 2BG. **EWW 253** on the reply card.

Sections on amplification, sampling, filter and oscillator circuits are included in the **TI bifet design manual** which also includes sections on individual devices and other circuits. Full circuit diagrams are included, with design equations. £3.95 + £1.50 post from **Texas Instruments Ltd**, PO Box 50, Market Harborough, Leices. **EWW 254** on the reply card.

The Sic Safco range of **paper, metallised paper and polypropylene capacitors** have uses in high and low voltage, d.c or a.c. applications. These high capacity devices are listed in a catalogue available from **Cetronics Components Ltd**, Hoddesdon Road, Stanstead Abbots, Ware, Herts. SG12 8EJ. **EWW 257** on the reply card.

ADU is an **autonomous data acquisition unit** described in a brochure from Mowlem. It is microprocessor-controlled and may be interfaced to a wide range of computers. Up to 255 channels may be monitored at one time and a process control module allows the control of motors. Further details from **Mowlem Microsystems**, Eastman Way, Hemel Hempstead, Herts HP2 7HP. **EWW 258** on the reply card.

Over half the **ECM catalogue** is devoted to components for frequency control; crystals, oscillators, filters and resonators. The other half lists semiconductors, capacitors, resistors, connectors and an assortment of other useful components. **ECM (Europe) Electronics Ltd**, Penmaen House, Ashington, W. Sussex, RH20 3JR. **EWW 259** on the reply card.

# Polyphonic keyboard — part 5

by D. J. Greaves B.A.

## Hardware details of Digipoly's two processors are presented in this final article.

The t.t.l. processor is clocked by a 10MHz Hartley oscillator using $Tr_6$ as the active component (December issue circuit). Output at 10MHz is converted to a squarewave using the self-biasing stage around $Tr_5$ and then divided by two by $IC_{36b}$ to give the operating frequency of 5MHz. This signal clocks the instruction address counter made from $IC_{2,10}$, as shown in October on the t.t.l. processor circuit.

Microcode for the processor is stored in $IC_3$, a bipolar programmable read-only memory (prom) from the MMI or Signetics 63xx series. The 6349 is organized as 512 locations of eight-bit bytes and has an access time of about 55ns; any non-volatile memory device with an access time of less than 150ns could be substituted.

Each op-code from the prom is latched in $IC_4$ while it is being executed. The four most-significant bits drive four-to-sixteen-line decoder $IC_5$, outputs of which select the operation.

Least-significant bits feed the data selector $IC_{12}$ to provide a page-select address for the processor's memory device, $IC_6$. Being n-mos, memory $IC_6$ is the slowest element in the t.t.l. processor and limits operating speed to 5MHz. Access time of this 2K-by-8bit static memory is 100ns. As can be seen from Table 1, which shows address allocations for $IC_6$, not all the memory locations are used.

The two 74LS181 four-bit arithmetic logic i.cs form the arithmetic unit. Accumulator output register $IC_{17}$ has its outputs permanently enabled in order to drive the A-bus. Together with the D-bus, the A-bus feeds into the a.l.u. where the two eight-bit numbers are combined to produce a new value for the accumulator.

Values for the D-bus are supplied from memory. The type of combination performed by the a.l.u. depends on the control number fed into the a.l.u. on pins three to six.

Arithmetic instructions in the t.t.l.-processor instruction set are ordered so that the a.l.u. control number can be derived directly from each op-code bit pattern.

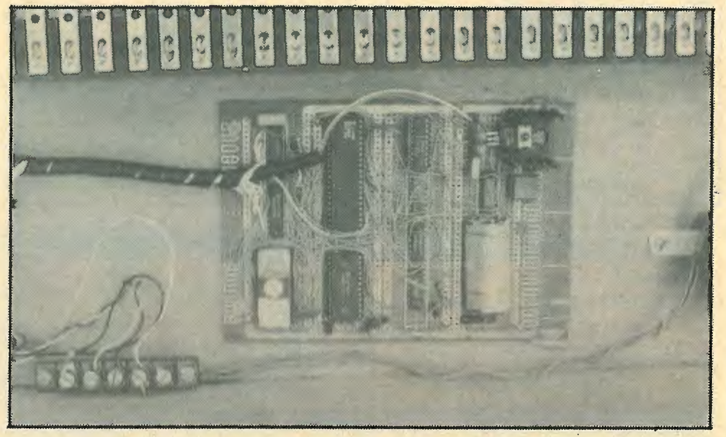
Bistable device $IC_{34}$ is a one-bit latch containing the carry bit. It is updated only as a result of an ADD instruction and its contents are fed into the a.l.u. through $IC_{33c,21d}$ during an analogue-to-digital conversion instruction.

For store operations, $IC_{16}$ is enabled to feed the accumulator value onto the D-bus so that the memory can be updated. Some store operations feed the output ports in an addressing mode decoded by $IC_{35c}$. One of two output ports is selected by $IC_{24}$.

Data for the output analogue converter is latched in $IC_{15}$ in two's complement form. Since the digital-to-analogue converter expects unsigned numbers on its inputs, $IC_{26c}$ adds 128 to the number which offsets the zero value to the middle of the converter's voltage range.

Addressing modes are decoded by random logic and determine what feeds the address inputs to the memory. Four-bit V-rigister $IC_{22}$ is gated onto $A_{0\text{-}3}$ by $IC_{13}$ if indexed addressing is required for V instructions.

Zeros are fed onto the low address bits by $IC_1$ and $IC_{11}$ feeds zeros onto the high address bits if indexing is not required. If accumulator indexing is required, buffer $IC_{18}$ is enabled to gate the A-bus onto $A_{0\text{-}7}$.



**8088 microprocessor board also contains an 8K eprom, 2Kbyte ram, an 8284 clock generator and crystal, NiCd battery for data retention, various support chips and an extra reset switch.**

Input to the t.t.l. processor occurs during the HOST instruction under control of the 8088 processor. The 8088 processor has an i/o bus called the Q-bus which feeds three register ports in the t.t.l. processor. Latches and operations of these three ports are shown on Table 2.

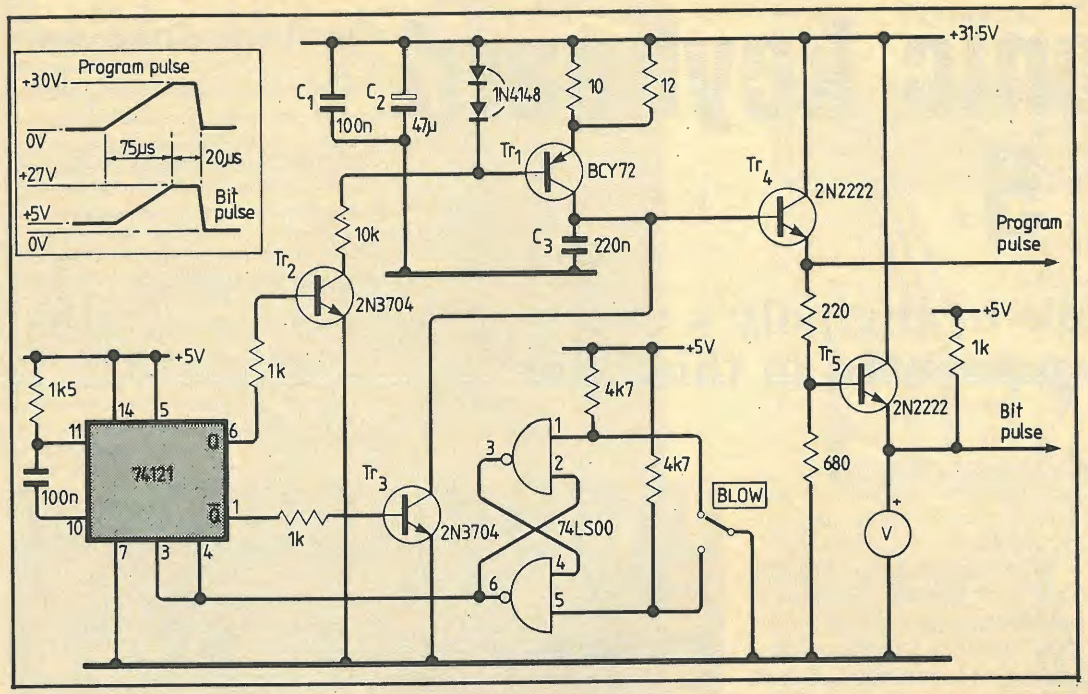
Writing data to port 14 also sets two-bit shift reigster $IC_9$ to all ones. Clocking of the shift register takes places at the end of each HOST instruction; if the output bit is one, data from $IC_{14}$ is written into the t.t.l. processor memory.

### Feature summary

Digipoly is an eight-note polyphonic digital musical instrument with a five-octave keyboard transposable over a nine-octave useful range. It includes

- Comprehensive envelope generator controls
- Vibrato and tremolo control
- Midi interface
- Hundreds of front-panel selectable waveforms
- Battery-maintained memory for 16 user-defined voices
- Rotary control for continuous adjustment of many parameters

Note frequencies are not rigidly locked as in divider type organs. A detune facility introduces a variable amount of scale error.



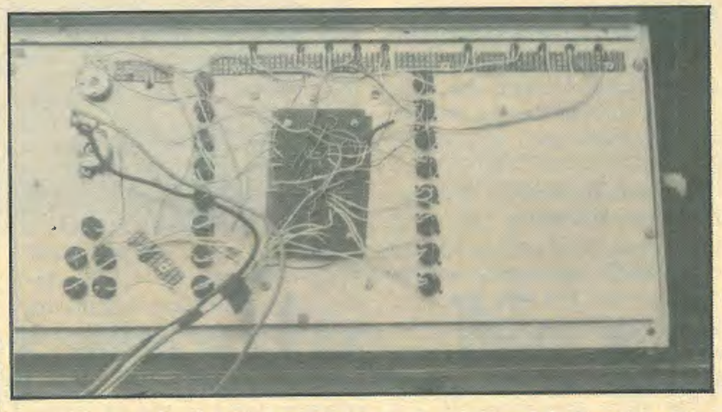

**Microcode for the high-speed t.t.l. processor is contained in a 63xx-series programmable rom (Monolithic Memories, Farnborough). This circuit, published on page 39 in the April 1985 issue of *Electronic Engineering* is for programming such roms. There are one or two minor errors in the previously published circuit.**

**The 6349 prom may be programmed manually by addressing a byte then using this circuit to program all bits that must be zero. The program pulse is fed to the chip-enable input, pin 15, and the bit pulse to the output pin.**

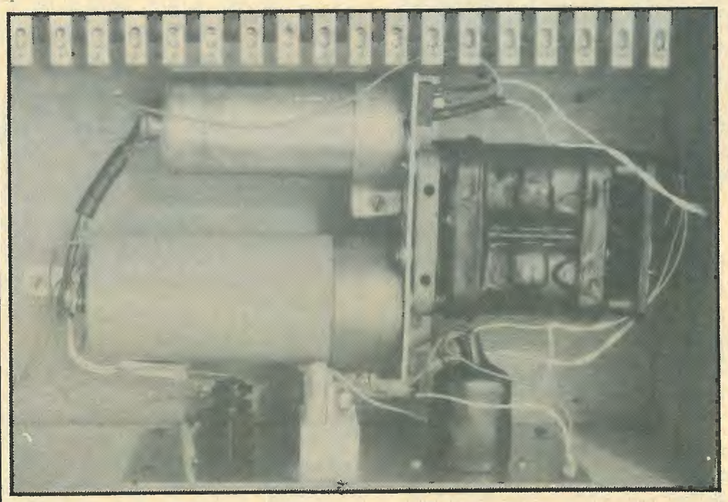
**Table 1. Memory use in the t.t.l. processor**

| Address | Array |
|---|---|
| 000-00F | low-order osc. phases |
| 080-08F | high-order osc. phases |
| 100-10F | low-order frequency values |
| 180-18F | high-order frequency values |
| 200-20F | volume values |
| 400-4FF | table of squares |
| 500-5FF | waveform table |
| 600 | $E_0$ register |
| 680 | $E_1$ register |
| 700 | $E_2$ register |
| 780 | $E_3$ register |

Note: the first five arrays are indexed using the V register; the two tables are indexed using the accumulator.



**Back view of Digipoly's front panel showing the knobs leds and switches. Four interface devices $IC_{47,48,49,63}$ are mounted on their own board, with led current-limiting resistors and the Q-bus terminating pull-up resistors.**



**Digipoly power supply provides 8V and −8V unregulated. Up to 2.5A is required from the positive supply to drive the 5V logic.**

Presence of the shift register causes the data to be written twice on successive HOST instructions. The second writing ensures that the correct data is written to the t.t.l. processor memory when the HOST instruction is executing at the time that the 8088 writes to $IC_{14}$.

For speed, and since the INCV instruction does not need access to the memory, INVC and HOST instructions are performed together using the same op-code. This is simply a matter of wiring outputs of $IC_5$.

The LOOP instruction causes the address counter to load a zero value on the next instruction. Since there is a one instruction delay through the prom and $IC_4$, the instruction after LOOP is always executed before control resumes at the start of the microcode. If needed, an accumulator indexed branch could be added by simply feeding the A-bus to pins three to six of $IC_{2,10}$.

## 8088 processor hardware

The 8088 microprocessor is mounted on a separate board with ten other i.cs, forming a self-contained microcomputer module. This module is connected to the rest of Digipoly through a single 25-pin connector carrying address/data lines for the 16 ports, signals for reset, busy and interrupt and an 8V supply line. This is a general-purpose computer board; I have used the same circuit in other applications.

Clock generator $IC_{50}$ is an Intel 8284 device. It divides a 14.7486MHz crystal frequency by three to obtain the two-to-one duty cycle required by the 8088 processor. Power-on reset and wait-state circuits are also provided by the 8284, although wait states are not used in this design.

Component $IC_{52}$ provides the 8088 processor with 2Kbyte of ram. This static ram is an HMM6116LP-3 c-mos device requiring only about 4μA of current in standby mode. It is practical to run the memory from a small NiCd battery for long periods; when Digipoly is switched on, the battery charges automatically from the 5V supply.

Supply-pin 24 of the ram is connected to the 5V supply but the ground pin is connected to ground through $Tr_8$. When the board is powered $Tr_8$ is switched fully on, bringing the main and i.c. grounds to within 50mV of each other. This figure is too small to affect logic switching. When power is removed however, $Tr_8$ turns off, causing the ram ground pin to move to −4.8V relative to the main ground.

Put another way, all ram control signals move to +4.8V, or logic one. Since the ram control pins are active when at logic zero, this disables the ram, putting it into low-power mode. When $Tr_8$ is off, its collector-base diode becomes forward biased so $Tr_7$ is needed to stop the battery being discharged through the base of $Tr_8$.

Input and output to the 8088 is performed through the Q-bus. This bus is a set of eight lines running through the whole instrument. Associated with the Q-bus is the MD-bus consisting of four lines for selecting one of the 16 i/o ports that the 8088 can address.

Both the MD-bus and the transceiver buffering the bus, $IC_{56}$, are set up before master strobe line GO is pulsed low. This gives time for written data to propagate and settle. On input cycles, the data is returned to the 8088 before the trailing edge of the GO pulse. This pulse is always about 350ns long.

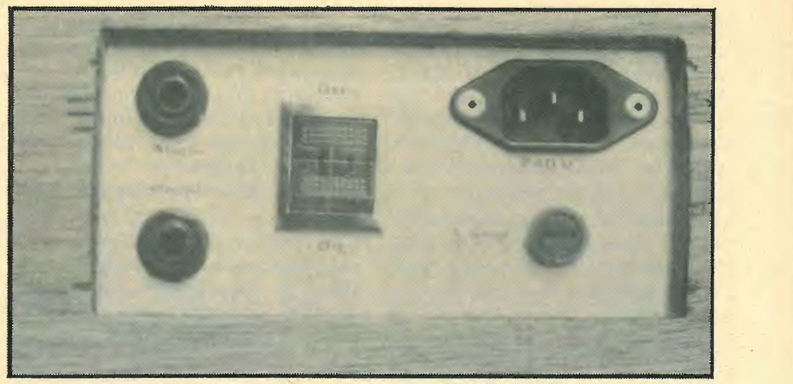
On arriving at the board, the active-low interrupt-request signal is inverted and fed to the 8088 maskable-interrupt input. The non-maskable input is not used. In response to an interrupt, the 8088 strobes INTA low twice at pin 24. The first strobe is a dummy one and the second reads an interrupt vector from the processor data bus. Eight diodes provide the vector by grounding each line during the acknowledge cycle, producing a zero value. Hence only vector zero is used and this sets software to read a serial byte from the Midi-in port.

**25-pin connectors** Two connectors, both D-types, link the main t.t.l. processor to the front panel and 8088 card.

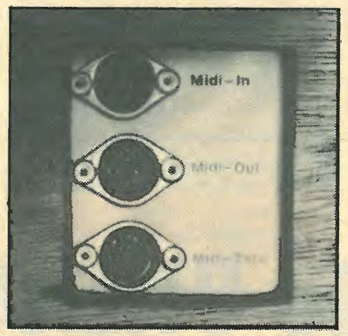
| Pin | 8088-board | Control panel |
|---|---|---|
| 1 | n.c. | 5V |
| 2 | 8V unstab. | n.c. |
| 3 | strobe, atc. low | read control buttons |
| 4 | ground | knob voltage |
| 5 | n.c. | pitch-bend voltage |
| 6 | $MD_0$ | read buttons 1-8 |
| 7 | $MD_1$ | read buttons 9-16 |
| 8 | $MD_2$ | write to leds |
| 9 | $MD_3$ | n.c. |
| 10 | $Q_7$ | $Q_7$ |
| 11 | $Q_6$ | $Q_6$ |
| 12 | $Q_5$ | $Q_5$ |
| 13 | $Q_4$ | $Q_4$ |
| 14 | ground | ground |
| 15 | ground | audio ground |
| 16 | BUSY | audio out |
| 17 | reset switch | reset switch |
| 18 | ground | ground |
| 19 | INT | n.c. |
| 20 | n.c. | n.c. |
| 21 | n.c. | n.c. |
| 22 | $Q_3$ | $Q_3$ |
| 23 | $Q_2$ | $Q_2$ |
| 24 | $Q_1$ | $Q_1$ |
| 25 | $Q_0$ | $Q_0$ |

**Table 2. Port data latches**

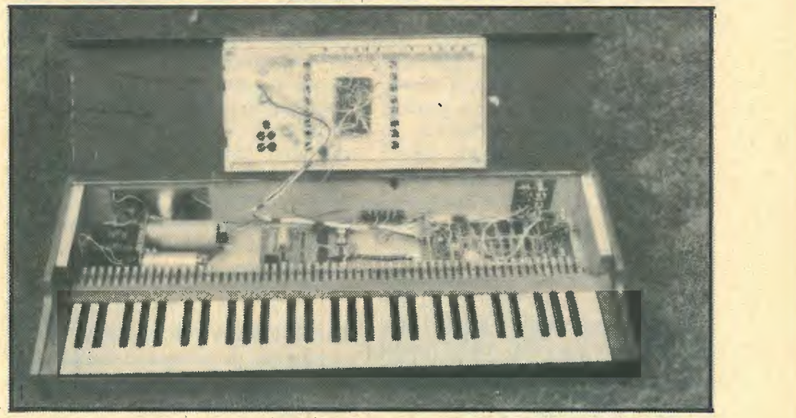
| IC | Port | Operation |
|---|---|---|
| 28 | 12 | select type of memory to be modified |
| 25 | 13 | memory offset of type defined above |
| 14 | 14 | data to be stored |



**Digipoly back panel provides an illuminated on/off power switch and access to the mains fuse. A BS4491 connector is provided for 240V a.c. input and 6mm jacks connect the sustain-pedal switch and the audio output.**




**Midi standard calls for three connections; Midi-in receives data which is automatically echoed on Midi-through. Midi-out leads to other devices under Digipoly control.**



**General view of Digipoly interior. The power supply is at the left, 8088 processor central and t.t.l. processor right.**

## Performance

Figure 6a in the September issue shows the Digipoly output spectrum when synthesizing a single 1kHz sinewave. The noise floor is at −65dB relative to the single note. This is virtually all sampling noise which disappears when no notes are pressed since d-to-a converter output is constant d.c.

Sampling noise can be heard quite clearly if Digipoly is connected into a high-quality amplifier and loudspeakers. This means that a further low-pass filter, for example on a mixing desk, has to be added before the sinewave voice can be used for quiet solo work. For all other voices there is no problem with output signal-to-noise ratio.

Owing to the note-generation technique, synthesis of high-frequency complex waveforms above about 1kHz is not good. Using higher frequencies, non-consecutive samples from the waveform table are taken with gaps of several samples. This causes small features in the waveform to become aliased, thus introducing the characteristically unmusical spurious frequencies into the sound. Remember though, that the true harmonics that these small features are supposed to add to the sound would be out of the audio spectrum and the desired sound can be achieved by using a simpler waveform.

Figure 6(b) in the September issue shows intermodulation product measured when two sinewaves are produced by holding down two keys at once. This product is presumably created in the 741-based active filter used in Digipoly's output circuit since the digital circuit behaves totally linearly. Figure 6c shows harmonic spectrum from a single squarewave.

Performance and versatility of Digipoly are very good. The instrument is capable of producing several well-known organ sounds, a good Fender Rhodes sound, good chime and bell sounds and a large number of rich, raunchy synthesizer sounds.

As usual with keyboard instruments, adding a few effects such as flanger and chorus can add a lot to the sound and the Midi interface puts the instrument among the best as far as interfacing goes.

**Complete Guide to Videocassette Recorder Operation and Servicing:** John D. Lenk. Prentice-Hall International, 365 pages, soft covers, £16.35. Technical details of a typical v.c.r. (Beta and VHS are covered) and a guide to trouble-shooting. As this is an American book, the circuit details relate to the NTSC system: European readers will need to do some translation.

**The Sinclair Story:** Rodney Dale. Duckworth, 184 pages, hard covers, £9.95. Sympathetic, though not wholly uncritical biography of the man who brought us the MAT100 micro-alloy transistor, the Black Watch, the pocket-calculator kit, the Microvision miniature tv set (several times), the ZX series of computers, the C5 electric buggy and many other epoch-making innovations. The author, one of the founders of Cambridge Consultants, traces Sir QLive's career from his days with *Practical Wireless* and Bernard Babani's publishing business to his recent flirtation with Robert Maxwell. Full of fascinating, nostalgic illustrations — advertisements, publicity photographs and cartoons — each one certain to evoke waves of emotion in all who cut their solid-state teeth on the likes of the Micro-6 radio (the world's smallest) and Sinclair's p.w.m. audio amplifiers. Highly diverting.

**Microcomputer Handbook:** edited by J.A. McCrindle. Collins, 622 pages, hard covers, £30. Comprehensive review of microcomputer technology and microcomputer systems, with chapters contributed by 26 authors from British and American companies and institutions.

**Television Engineering, part 1: Fundamentals:** edited by R.S. Roberts (Royal Television Society). Pentech Press (marketed by John Wiley & Sons), 259 pages, hard covers, £24. Authoritative textbook based on the RTS's own television engineering course. Contributors are drawn from Marconi, the BBC, Thames Television and others. Subjects include basic principles, modulation, digital techniques, transmission standards, filters, colour, video processing, receivers, pulse and carrier generation, timing a colour studio system, the camera and camera tubes. Part 2 (after the break, no doubt) will deal with specific engineering applications.

**Wordwise Plus:** Bruce Smith. Collins, 239 pages, soft covers, £9.95. Wordwise Plus is the latest version of the BBC Micro's biggest-selling word-processor. This treatment is by the technical editor of Acorn User who pitches it at a level suitable for the total newcomer to computing. However, the manuals that come with Wordwise Plus itself are unusually good and leave him little scope to improve upon them. The most interesting section is that on Wordwise Plus's built-in text-processing language: sixteen example programs are given.

**An Introduction to Computer Peripherals:** R.A. and J.W. Penfold. Bernard Babani BP170, 65 pages, soft covers, £2.50. Printers, plotters, monitors, modems, mice and mass storage devices: how they work, and how to connect them up. Useful tips for the newcomer. A section on interfaces briefly explains the RS232 and Centronics standards.

# BBC MICRO UTILITIES

The BBC microcomputer has now been in circulation for four years. The original 16K and 32K models are no longer in production in Britain; yet although their successors may have been overtaken in the eyes of marketing men by 16-bit machines, the reliability and versatility of the BBC design have won it a place in laboratories everywhere. And the quality of some of the software now available for the BBC micro seems to assure its position for some time to come. Below is a selection of recent utility packages.

**Machine code monitor:** the BBC's own monitor has been a long time in coming but is undoubtedly one of the best. Facilities are very easy to use and comprehensive too, lacking only the dual-screen feature of Beebugsoft's Exmon II. The memory editor scrolls less smoothly than some, but can access any byte including those in paged roms and in the 6502 second processor.

The disassembler copes with 65C02 op-codes and it labels over 50 system calls and vectors with their proper names. Further labels supplied by the user can be loaded from disc or tape.

A single-pass assembler is built in, but a full disc assembler is supplied on the accompanying utilities tape. The tape includes some other useful items, among them a pair of disc sector editors for the Acorn DFS and ADFS; a file enabling Monitor to be used with the AMX mouse; a second-processor version of Monitor; and a program which enables the program-tracing output to be sent to another computer via the serial port. Monitor, from BBC Publications, is suitable for BBC models A, B or B+, comes in 16K of eprom (plus a tape, transferable to disc) costs £39.95 including v.a.t. **EWW 240** on the reply card.

**Inter-Chart** line-graphs, bar-graphs and pie-charts are made easy by this rom package from Computer Concepts. Data can be entered at the keyboard or imported from other sources, edited if necessary and then displayed in colour, saved or printed. Scaling of the graph takes place automatically on the screen. Sixteen graphs (or even more) can be held in memory at once, different ones can be overlaid if necessary and the form of the display can be changed at any time.

Interchart is one of a series of roms designed for easy interchange of data between one application and another. A database and word-processor are promised, but already available is an exceptionally powerful spreadsheet; **Intersheet** Sheet size is 64 boxes by 255 and the screen width can be switched to 40, 80 or 105 columns. The formulae relating one box to another can include a comprehensive range of mathematical functions, including some not available from Basic such as counting and averaging. Calculation is very fast. Inter-chart costs £36.80 including v.a.t.; and Inter-sheet, in two roms, costs £56.35. Computer Concepts, Gaddesden Place, Hemel Hempstead, Hertfordshire HP2 6EX. EWW 241.

Basic compiler: **Accelerator,** the compiler from Computer Concepts is not quite as useful as it sounds. Although compiled code can can never be as fast as hand-wrought machine-code, Accelerator certainly provides worthwhile speed increase over the standard BBC Basic interpreter. But restrictions on its use mean that many existing programs cannot be handled by it without modification.

Accelerator compiles the Basic program in memory, or on file, first to an intermediate code called G-code. This code is interpreted at run-time by one of the two roms in the Accelerator package. With some types of program, G-code can show a five-fold increase in speed: those involving heavy calculations seem to benefit most. But others, such as graphics routines, may show little improvement. A G-code version is roughly the same length as the Basic original and it may be run directly, or saved, or — for an additional speed increase — compiled further to full machine-code.

However, there are certain Basic words which for various plausible-sounding reasons the G-code compiler does not accept. These include Eval, Page, Lomem and the assembly-language instructions built into BBC Basic. Chain, Fn and Rnd are handled in a way different from the usual one. And the machine-code converter (supplied on disc, together with some utilities and example programs) cannot compile floating-point arithmetic. So logarithms, pi and trigonometry are all out-of-bounds.

Another snag with the converter is that it stores integers in two-byte form rather than the four-byte form of BBC Basic. Difficulties can therefore arise with negative numbers and with the 12-bit Basic Adval function.

These limitations may sound alarming, though for many purposes they need raise no problems if the source code is written with Accelerator in mind. The manual, which is well-written, is quite candid about them. Accelerator costs £64.40 by post. **EWW 242** on the reply card.

## Eprom programmer software

Norman Sargent tells us that line 2530 in his program enhancement should read DEFPROCdisible and not PROCdisible. This enhancement on page 85 of the November issue is for software to run John Adams' eprom programmer from the BBC microcomputer.





## Natural ELF antenna

Ever since the experiments carried out by RCA in 1966-67 when it was shown that worldwide communications was feasible on frequencies below 100Hz there has been growing interest in exploitation of the e.l.f. band of 3 to 3000Hz.

"Project Sanguine" of the Lincoln Laboratory (M.I.T.) and "Project Seafarer" confirmed the extremely low attenuation of 45Hz and 75Hz signals propagated in the Earth-ionosphere waveguide, but also emphasised that the major problem was the enormously long antennas necessary at these wavelengths to radiate even a tiny part of the energy fed to the antenna. In Project Sanguine maximum radiated power was not more than 0.5W at 45Hz, 1W at 75Hz but decodable signals were received in Norway, Malta, Saipan and Hawaii using modest air-core loop receiving antennas. Attenuation of signals can be as low as 1.5dB over 1000km.

Apart from needing antennas many miles, or even hundreds of miles, long, a practical snag is the very low bit rate that can be achieved. In Project Sanguine this was as low as 0.03 bit/second though in an operational system about 1 bit/second is feasible. The U.S. Navy has an e.l.f. station in Wisconsin on 76Hz, taking advantage of the ability of such signals to penetrate well below the surface of the sea for reception by submarines.

A new twist has been given to the exploitation of e.l.f. by showing that it is possible to use the Earth's atmosphere as an antenna, for example by modulating the conductivity of the polar electrojet.

As reported in *Nature* (September 12, 1985) this has been achieved experimentally by operating the high-power ionospheric heating transmitter (270 megawatts on 2.759MHz) at Ramfjord, near Tromso in Northern Norway, sinewave modulated at 1.57kHz or 1.04kHz.

As a result of the ionospheric non-linearity this resulted in variable r.f. output at 1.57 or 1.05kHz ranging from under 100 microwatts to over 2 watts radiated from the electrojet and successfully received at test sites 205 and 554km from Ramfjord with attenuation of between 5 to 30dB/1000km.

The use of ionospheric heating transmitters in this way makes it possible to tap into enormous natural power sources. The technique of increasing the electron temperature of the ionospheric layers to permit extended range of v.h.f. signals by field-aligned scatter techniques has led to the development of high-power ionospheric heater transmitters. Whether their use can be extended to practical e.l.f. systems remains to be seen.

## Crystal Palace

In his presidential address to the IERE "Fifty years of high-definition television transmission" Raymond Hills brought to light many details of the original Baird and Marconi-EMI transmitters installed at Alexandra Palace in 1935-36. But, perhaps wisely, he steered clear of the controversy and bitter feelings that surrounded not only the failure of the two companies to agree on a single "standard" but also the choice of Alexandra Palace for the London station. Even in 1935 it was recognised that the Crystal Palace in South London was a technically superior site but had been pre-empted by the Baird company who proceeded to use the building not only as development laboratories but also (at least in the view of the Post Office and BBC) to set up the studios, dressing rooms etc that would be required for a London television service.

When the Post Office people saw the extent of the Baird Crystal Palace facilities it reawakened the fears that had haunted them ever since 1926. The then current Wireless Telegraphy Acts did *not* cover the transmission of visual images. Their legal people had wanred that there was nothing legally to stop Baird from setting up in the UK his own television service providing that he did not broadcast a sound channel! The cinema had established itself successfully in the "silent" era, 1910 to 1930, so the idea was not as far-fetched as it may appear today. The public would soon demand that the Baird company would be given a licence for sound.

The Baird Company, the controlling interest of which had by then been taken over by the Ostrer brothers, the cinema magnates, attempted to win public and political support before and during the Selsdon inquiry on the grounds that EMI was American-controlled (actually RCA had a 27% shareholding) and used Anglo-American technology whereas the Baird system was "all-British". Both companies had been asked to refrain from press publicity until the Selsdon Committee reporte,d but this agreement was frequently broken.

A bitter series of complaints led (Sir) Isaac Shoenberg to write, on December 27, 1934, an irrate note (copy in Post Office Archives) to Varley Roberts (P.O. secretary of the Selsdon Committee): "Nobody could, in fairness, possibly think we could have anything to do with a statement which called the Baird system 'All-British' when it is known to everyone that the greater part of the apparatus for that system has been obtained from Germany; of which company the American Fox Films own 50 per cent; nor with a statement that designated our system 'Anglo-American' when, as you are well aware, our television has been developed in our laboratories here."

Shoenberg went on to claim that "we have not indulged in a single publicity stunt during the whole development of our system" — ignoring the visit of King George V to Hayes that month and an earlier demonstration of the EMI system at Windsor Castle. At that time both EMI and Baird were demonstrating 180-line systems, both without interlace. Shoenberg's letter carries a diplomatic comment by Roberts to Lord Selsdon; "I think if you agree these papers might be registered and put away." No mention.

The later Television Committee, set up after the Selsdon report, visited Crystal Palace but opted for Alexandra Palace, and agreed that 405/240 line standards when they failed to persuade Marconi-EMI and the Baird Company to agree a common standard as had been envisaged by the Selsdon Committee.

It was soon after the start of the dual-standard service from Alexandra Palace in November 1936 that the main part of the old Crystal Palace, other than the tower housing the Baird laboratories, was destroyed in a fire that could be seen for miles. So vanished the studios that may or may not have been intended to provide the London television service! It was never clearly established how the fire had started, though some suspected arson.

## Survival?

Coming, as it did, the day after it was finally confirmed that the Pentagon would buy Rita rather than Ptarmigan, the 1985 Mountbatten Lecture of the National Electronics Council by Basil de Ferranti, chairman of Ferranti, plc and M.E.P. for Hampshire Central on "Electronics, Europe and Survival" seemed to promise more than in fact it provided.

Basil de Ferranti delivered a polished, logically-presented argument in favour of a large European market in which salesmen and lorries could move more easily and more cheaply if only the airline cartel, the frontier documentation, customs delays, V.A.T. differentials and nationalised industries could be eliminated or minimised and/or computerised and privatized.

He argued that the USA had prospered by having a home market of over 200-million people — and that Europe could do the same. He did not spoil his argument by explaining how Japan has grown to dominate European electronics, without a 200-billion plus home market — or why the American electronics industry now fears Japan.

Not unnaturally he instanced the way in which Ferranti, who took the computer to the marketplace ahead of the world, was soon overtaken by IBM because of the much larger American market.

It would indeed be convenient to hang the problems of the British communications and electronics industry on this one peg of market size — but surely misleading. Equally to blame, I would suggest, is the perennial and rather arrogant British belief that we have the best scientists and engineers but who are let down by their marketing people. The difficulty with major projects like System X and Ptarmigan is the time it has taken to get them into production and to eliminate the software bugs, while repeatedly tacking on later bits of new technology. We still have not learned the lesson of "keep it simple, stupid" and "pioneering don't pay". Its better to come second with a simple, bug-free product, and forget the "not-invented-here" syndrome.

It may also be time for the N.E.C. to decide in what direction the annual Mountbatten Lecture should go. The eight so far have had no common central theme or discernible purpose. A few brilliant, some pedestrian and some overtly political. As major occasions, chaired by the Duke of Kent, they seem to lack something.

## Here and there

Misprints, unhappily, we all have to live with. But an unfortunately misleading error crept into my November item on "Friendly r.f." This gave the success rate of pulsed l.f. waveforms used to heal difficult bone fractures as "close to 8%". It should have been the very different figure of "close to 80%", even though, as the Americans pointed out, "the bone fractures of patients selected for this treatment had generally failed to heal over months or even years — often despite repeated surgery". In one trial at Columbia Presbyterian Hospital a success rate of 93% was achieved, rising to 98.5% after a second round of treatments, with no known adverse side effects. Many of these patients had been disabled for several years and seemed destined for permanent disability.

The BBC2 200kHz long-wave station at Droitwich is now using its new 500kW transmitter with two new 700 ft masts. The frequency will be changed at 198kHz during 1988, a point to be noted by all who use this station as a high-stability source.

# Amateur Radio

## Slower growth

The decline in the number of youngsters becoming interested in the hobby of amateur radio, other than as a means of linking personal computers together, is reflected in the R.S.G.B. review of the year to June 30, 1985.

This shows that while membership has risen from 35,860 to 37,096 during the year, the number of new members has declined sharply since the peak of 5737 in 1981-2 to 5,501 in 1983-4 and 4,310 in 1984-85, with just over 3,000 members dropping out this year.

The Society has managed to reduce its financial revenue deficit for the year from £50,242 to £30,720.

The DTI have more clearly defined the conditions under which Class B (v.h.f.) licensees may work "cross-band" to amateurs using h.f. bands, including satellite transponders on the 28MHz band. The RSGB is also pressing that 50MHz, when this band is generally released, should be available to Class B licensees. The Society is also urging that the Radio Investigation Service should take more active steps to stamp out "spectrum abuse", labelling the service as grossly inadequate.

It is noted in the report that many television receivers which meet the requirements of BS905 and experience no problems from local h.f. transmissions, nevertheless suffer severe breakthrough when near 144MHz s.s.b. transmitters of more than about 10 watts p.e.p. output.

The number of QSL cards passing through the Society's QSL Bureau is put at 2.4 million, about the same as last year.

The 55 national societies of the I.A.R.U. Region 1 Division had some 170,000 licensed members in the 1985 tally, an increase of about 7,500 over 1984. West Germany (DARC) has the largest number 39,378; followed by RSGB 28,892, Spain (URE) 12,495, and USSR (RSF) 11,429. Several societies, however, have reported a decrease in licenced members including France (REF), Holland (VERON) and Belgium (UBA). For example of 5,651 licensed amateurs in Norway, 3,691 were members of NRRL, a reduction of 200 in the year to April 1985.

## From all quarters

The third space shuttle mission, Challenger 61-A carrying three radio amateurs was launched on October 30. Many of the amateur-band transmissions from this craft were made automatically with incoming cross-band signals recorded on-board Challenger for later analysis.

- The FCC has released to American amateurs the frequency band 902 to 928 MHz band which they will share with industrial, scientific and medical users. Japanese transceivers designed for their 903 to 905 MHz "personal radio service" (no legal 27MHz c.b. in Japan) which has not proved as big a market as expected, are likely to be used by amateurs in the USA.
- During 1985 two Swiss amateurs, HB9AMH and HB9MIN, established a new amateur millimetric-wave record, with a two-way contact on 47 GHz over a distance of 53km using portable tripod-mounted 10mW Gunn-diode oscillator transceivers (HB9AMH's had 23.5 GHz fundamental with Schottky-diode doubler/mixer). Antenna dishes were first aligned using 24 GHz Gunn-transceivers.
- The Belgian PTT has formulated new restrictions that would limit maximum transmitter output on 144 MHz to 50 watts, abolish access to the 5.7 GHz band and reduce the width of the 430MHz, 1.3 and 2.3 GHz bands.
- American amateurs are increasingly concerned at the poor shielding and plastic cases of domestic VCR machines that make playback heads suceptible to strong local signals in bands below 7 MHz.
- Grant Dixon, G8CGK has reported in *GQ-TV* general loss of sensitivity of amateur tv receiving/converters using BFR34A input transistors. Although the likely cause is static build-up this more commonly results in sudden catastrophic failure of unprotected front-end devices. American amateur-TV enthusiasts are concerned less proposed band-sharing of 421 to 430MHz with land-mobile radio could threaten ATV in the USA. The section 420-430MHz is no longer available to amateurs within 50 miles of the Canadian border.

## Morse and the deaf

Nigel Neame, formerly G2AUB, became interested in radio as a young schoolboy at a time when it was possible to buy or devise components and build receivers and transmitters within the budgetary limitations of "pocket money", aided by the weekly technical radio magazines that sold for a few pennies. He belives that entry into the hobby today has become altogether too costly and too dependent on factory-made equipment. Schoolboy enthusiasts of the 1930s often found a career in radio.

But his main plea is concerned with his own handicap of deafness. He believes that communication by morse code is one of the few ways in which the deaf can communicate with other people "on equal terms". He has proved that even the severely deaf can read morse signals with the aid of audio filters (or even vibrating sensors) and that every effort should be made to teach them morse code and to encourage the construction of simple transmitters and to provide low-cost cw-only licences etc.

**Pat Hawker, G3VA**

# 68000 board–4

by R.F. Coates

## With the board now working and talking to the terminal Bob Coates turns to his Kaybug monitor software.

The monitor has been made as friendly as possible. It prompts the user for the next entry line where necessary and gives a 'help' listing which shows all the available commands with a brief description of each. Even the occasional user should not need to refer to the full description having once studied it.

A total of 38 different commands is available, each one invoked by a simple two-letter code. Any further information required is prompted for. The commands allow listing of memory blocks, altering memory, loading object code from host, setting breakpoints, altering register contents, running programs, single-step tracing through programs and so on.

The monitor accepts either upper or lower-case letters. Printing on the terminal screen is formatted to suit 80-column terminals but a command allows an alternative 40-column format.

There is a collection of system calls (sub-routines) which a user's program may call upon. Most are concerned with reading the keyboard and writing to the terminal screen, but others include b.c.d. to binary conversions and a 32-bit divide.

Unless otherwise stated, addresses and values entered are eight-digit hex numbers. The last eight are taken if more than eight are entered and leading zeroes are inserted if there are fewer then eight. Addresses must begin on word boundaries (even addresses).

### The command set

**An** — *examine/alter address register:* the value in any of the target program's processor registers may be examined and altered if required. This command applies to the address registers $a_0$ to $a_6$ ($a_7$ is the stack pointer).

The command is invoked by keying the letter A followed by the appropriate number from 0 to 6. The current contents are then displayed (zero after a reset). The user is asked to enter either a new value followed by <cr> or just <cr> to leave the contents unaltered.

**AE** — *Ascii entry:* if text strings are to be included in your program, this command allows them to be entered more easily than is possible with the *MO* command.

It asks for the starting address and then waits for Ascii characters to be entered. It stores them as a string of bytes in memory. All Ascii characters and control codes are stored, apart from the break/hold characters and the following —

Backspace: does not store but backspaces the memory pointer and terminal cursor to allow corrections to be made.

Control-C: stores 'carriage return' with bit 7 set ($8D_{16}$).

Control-L: stores 'line feed' with bit 7 set ($8A_{16}$).

Control-N: stores null (00), the terminator required by *pdata1/pdatam*. Displays as \0.

The terminator control code set by *ST* is used to exit the *AE* command, the address following the end of the string being displayed.

**AS** — *line-by-line assembler:* This is an optional extension to the monitor.

It accepts assembler source code a line at a time, assembles it and stores the resulting object code in memory.

When this command is invoked, the display shows the default starting address which is $400400_{16}$. If a different address is required, the new address may be entered in hex, preceded by a dollar sign.

| Kaycomp specification | |
|---|---|
| Processor | Motorola MC68000 or MC68010 |
| Data bus | 16 bits |
| Clock speed | Up to 10MHz |
| Eprom | Up to 128K-bytes |
| Ram | Up to 64K-bytes |
| Serial i/o | Two RS232 ports, 75 to 19200 bit/s |
| Parallel i/o | 26 i/o; six input; six output |
| External bus | G64-bus (peripherals) |
| Dimensions | 233.4mm × 160mm (double Eurocard) |
| Power | +5V at 0.7A, +12V and −12V at 30mA |
| Firmware | Comprehensive monitor<br>Line-by-line assembler |
| Cost | Bare board: £18.90; with eproms and monitor, £34.40; with assembler too, £48.40; from Magenta Electronics, 135 Hunter Street, Burton-on-Trent, Staffordshire DE14 2ST. All prices include v.a.t. Postage costs 60p extra. |

Each assembler source line should be terminated by a carriage return, e.g.

moveq #10,d3<cr>

After the terminating carriage return, the line is assembled, object code stored in memory and the line displayed as follows,

400400 760A moveq 10#,d3
400402

indicating the address, the object code produced and the original input line.

Lastly the address is incremented and displayed on the following line to await the next entry.

All standard Motorola instruction mnemonics are accepted as well as the five pseudos *$nnnnnn, data, ascii, asciz* and *end.*

*$nnnnnn* alters the working address to nnnnnn. The address entered must be even.

*data* allows bytes of data to be entered, e.g.

data 0,1,$10,32

will enter hex bytes 00, 01, 10, 20 into memory.

*ascii* allows Ascii text strings to be entered. The pseudo *ascii* must be followed by one space. All keys entered, up to the terminating <cr>, are then stored in memory as Ascii characters.

*asciz:* as *ascii* but also appends a null byte to the string, as required as terminator by *pdata1.* Note that if an odd number of bytes are entered with the *data, ascii* or *asciz* pseudos, then if an instruction mnemonic follows, its code will automatically be aligned on the next word boundary.

*end* terminates the assembler command and returns the monitor prompt. The <del> key will also abort the assembler, as with other commands.

Instructions for the 68000 can be specified as one of three sizes: byte (.b), word (.w) or long-word (.l). The required size specification is appended to the mnemonic, e.g.

eor.b d3, (a6)

If no size is specified then 'word' is assumed.

Some instructions allow only one size. In such cases, no size may be specified.

Most of the addressing modes are as standard Motorola assembler format, but some variations should be noted (see box, right).

Since the assembler works line-by-line it has no way of resolving labels. Branch destinations must therefore be entered either as an absolute address,

bra $400426

or as a p.c. relative displacement,

bra * +26

(branch forward 26 bytes)

The displacement may be either short (8 bits) or long (16 bits) and is specified by appending .s or .l to the mnemonic. If no size is specified, .l is assumed:

bra.s $400426

(one-word instruction) or

bra.l $400426

(two-word instruction).

### Addressing mode details

**Indexed**

The size subscript for the indexing register is optional, 'word' being the default.

**Absolute word/long**

This may be entered either as an absolute address or as a displacement from the current address. It must be suffixed with wither .w or .l to indicate absolute word or absolute long modes. So

400400 clr $400420.l and 400400 clr *$20.l

are equivalent instructions (*means current program counter contents).

**P.c. relative, indexed**

The format of these is similar to 'register indirect with displacement' and 'indexed', but with 'pc' replacing the register. The interpretation of the displacement is different though:

movea 10(pc), a6

means the displacement will be the relative offset between address 10 and the current address.

movea * + 10(pc), a6

means the displacement will be the relative offset between the current address + 10 and the current address: in other words, 10.

In the case of the line . . .

lea string, a6

(which loads a6 with the relative address of label 'string' at assembled address of $$40043C_{16}$, the line would be entered as lea $40043c(pc), a6

**Bn** — *breakpoint display/set:* up to four separate breakpoints may be set within a program, B1, B2, B3 and B4. If, say, B1 is entered, the terminal displays the address where this breakpoint is set. The user may either hit just <cr> to leave the breakpoint set at the current address; or else enter a new address where the breakpoint is to be set, removing any old breakpoint that may be set. If an address of zero is entered then no new breakpoint is set, just the old one removed.

**CM** — *compare two blocks of memory:* this command compares two blocks of memory and prints any differences between them. It asks for three addresses to be entered: the start address of the first block, the end address of the first block and the start address of the second block. It then compares the memory blocks byte-by-byte and prints a list of addresses (first block address given) where bytes do not match.

**CN** — *continue execution after break:* when a breakpoint is set at a particular address in ram with the *Bn* command, the original instruction at that address is saved and replaced by a Trap instruction with vector number 15 to 12 for B1 to B4 respectively.

When this instruction is executed the processor jumps back into the monitor, first displaying the current status of all the registers. If it is now desired to resume execution from this point, the *CN* command will re-start the program by re-inserting the original instruction at the breakpoint address and running that instruction. Thus the breakpoint is automatically cancelled by this command.

**CV** — *convert between hex and decimal:* this useful programming aid will convert numbers from hexadecimal to decimal and vice-versa.

To enter a number in hexadecimal form, prefix it with the letter X. The largest number that may be converted is 99999999 or its hexadecimal equivalent.

**Dn** — *examine/alter data registers:* this is exactly the same as *An*, but works on data registers $d_0$ to $d_7$.

**FI** — *fill block of memory with word.* The start and end address of the memory block are requested first, then the value of the data word (up to four hex digits). The memory block is then filled with this word.

No checks are performed to see whether the data has been stored correctly.

**GO** — *go and execute target program:* this is the command to start running your target program. It asks for the start address of your program, then sets all the processor registers to the target values (as shown by *RD*). It then loads the program counter with the entered address, transferring control to your program, in which it will remain until a breakpoint, say, returns it to the monitor.

**HE** — *help:* gives a brief description of all commands.

**LH** — *Load S file from the host into memory:* this is used to download an object-code file created by a host computer's assembler or compiler into the Kaycomp's ram area ready for running. The host system must be capable of outputting the object file in the standard Motorola S2 Ascii format.

The *LH* command is very similar to the *TM* command, the Kaycomp going 'transparent' and the terminal being able to talk to the host computer. In addition, though, it looks at the information coming back from the host for data in S file format, which contains Ascii encoded object code plus address and checksum information. If it finds this, it will decode it and store it at the designated address in memory.

If an error occurs during loading — if a byte is not stored correctly or if there is a checksum error — then the message

*** LOAD ERROR ***

will appear and the command will be aborted.

If the S file is loaded in correctly, the end-of-file marker will cause the command to exit without error. Alternatively, an exit from the command can be forced with <control-T> or whatever the terminator has been set to by the *ST.*

If a breakpoint is set in memory at a point where *LH* loads new data, then the breakpoint is cancelled.

The procedure then for using this command is first, key *LH*; key in the host system's command for dumping an object file in S format; then wait until the file is loaded (it is displayed as it is received).

**LT** — *Load S file from terminal:* this is the same as *LH* except that it receives the S format file from the terminal rather than the host port.

After this command has been entered, the computer being used as terminal must exit terminal mode and be made to download the S file.

**LW** — *locate data word in memory:* this will search for a particular data word in a memory block.

It asks for memory block start and end addresses and then for the four-digit hex data word to be located. It will then print a list of all addresses in the block where the data word is found.

**MO** — *memory open/modify:* this command allows you to examine and modify memory a word at a time.

It first asks for the address where you wish to start. It then displays that address and its current contents.

The user may choose to alter the contents by entering a new four-digit hex value.

The line should be terminated by one of the following keys:

(a) <space> will cause the new data word, if entered, to be stored in memory. The command will then step on to the next memory word.

(b) <∧> (upward arrow on some terminals) causes data to be stored and then the previous word opened.

(c) <cr> causes the data to be stored and the command exited.



If a new data word is stored, a check is made to ensure that it is stored correctly (i.e. addressed to ram and not to eprom).

If it has not been stored,

*** NO CHANGE ***

is displayed and the command exited.

**MV**— *move memory block:* allows a block of memory to be moved up or down in memory by as small or large a shift as required.

It asks for the start and end address of the memory block to be moved and then the new start address it is to take. No checks are performed to see whether the bytes moved are correctly stored.

**PR** — *Print memory block:* prints on the screen the contents of the specified block of memory.

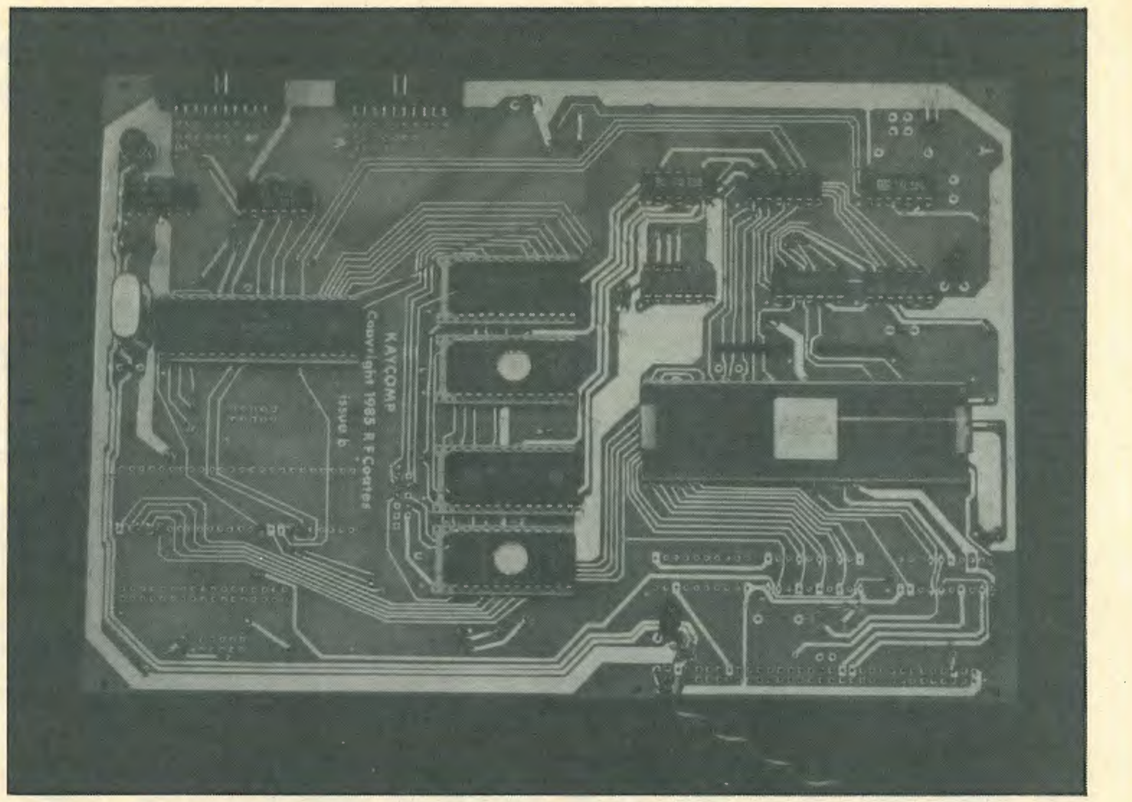
It asks for the start and end addresses of the data block (which need not be at word boundaries as the start address is rounded down to the start of a 16-byte block and the end address rounded up). In asking, it displays the value last used and re-uses it if you hit just <cr>.

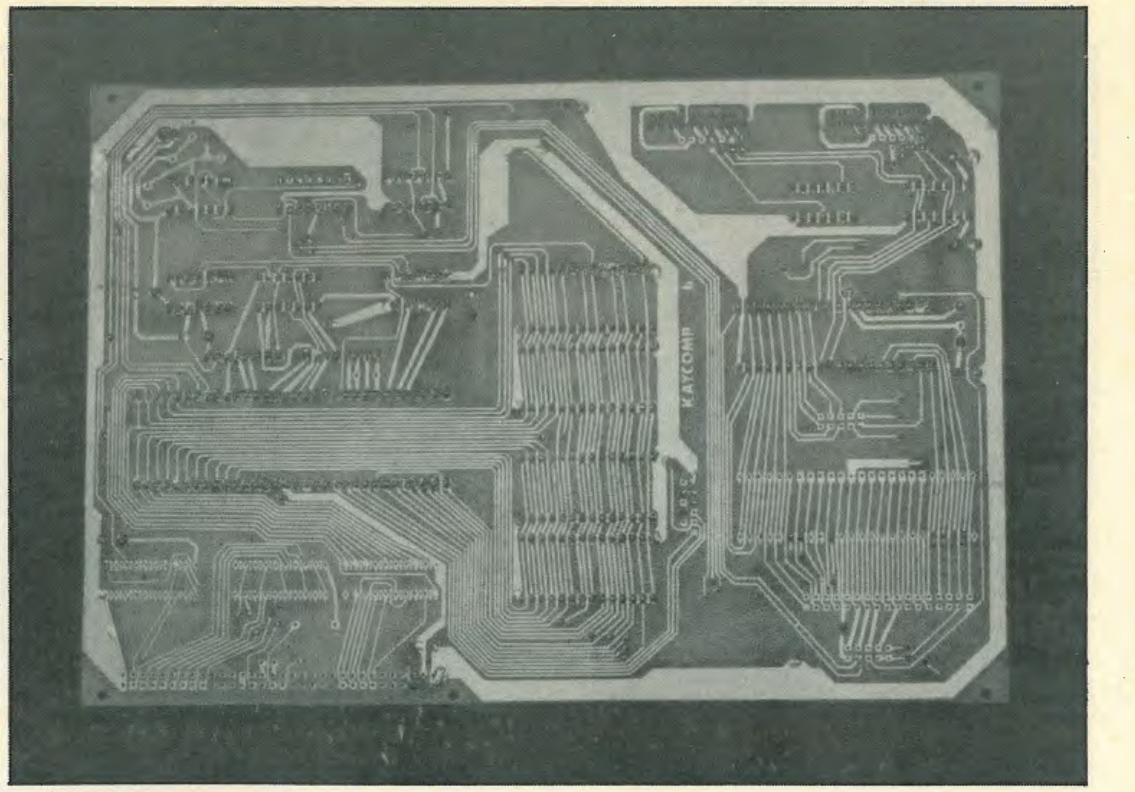
The data is formatted into word-sized groups. Eight words are displayed to a line in the 80-column mode (see *TC*), four words per line in 40-column mode. On the right of each line is displayed the Ascii equivalent character of each byte in the line (a dot if there is none).

Control-S and control-Q may be used to control the output, <del> to abort it.

**RD** — *Display target program's registers:* this command is called automatically when a breakpoint is encountered. It shows the contents of all the 68000's registers. The values displayed are those which the registers will contain if a program is started using *GO* or re-started using *CN.*

With the exception of the status register (SR), all are 32-bit registers and are displayed as eight-digit hex numbers. 'A7' refers to the supervisor stack pointer, as Kaycomp always operates in supervisor mode to allow the user unhindered access to all instructions except when a user's program switches the processor to the user mode.




The status register is only 16 bits in size. If it were displayed as four hex digits, some mental agility would be needed to discover the state of each individual bit. The status register is therefore displayed as 16 individual bits: a 1 indicating bit set, 0 bit clear. Each allocated bit is labelled by a legend above.

The program counter (PC) is the address where the breakpoint trap instruction was encountered.

**SR** — *examine/alter status register:* equivalent to *An* but operating on the status register.

It accepts and displays a four-digit hex value; so the particular bit pattern required must be converted to hex before being entered.

**Correction:** in the December article, the ninth line on page 38 should begin, "If power is *not* derived..."

**ST** — *set terminator.* The *LH, LT* and *TM* commands may, by default, be terminated by keying <control—T>. However, this particular character may have some function on the host computer you happen to be using and so there might be no way to send this code through from terminal to host.

To overcome this problem, the command *ST* allows the terminator to be changed to some other control code. This may be any Ascii control code (00 to $1F_{16}$) other than carriage-return ($0D_{16}$).

**TC** — *toggle column mode.* The displays associated with some commands assume that an 80-column terminal is being used and make full use of the screen width available.

This presents a problem where the terminal has fewer than 80 columns, for instance, a home computer with only 40 columns. But the command *TC* causes 40-column print formatting to be used in all subsequent operations. Entering *TC* again will switch back to 80-column mode.

**TR** — *trace target program:* when your program does not work and you cannot find where it is going wrong, it can be helpful to step through it one instruction at a time.

*TR* allows this by executing the target program and after each instruction displaying the register contents as with *RD*. It will continue this until a breakpoint is hit or control is passed back to the monitor, but control—S can be used to suspend execution and display.

*TR* asks first for the address where tracing is to be started; then for the address where the program is to be started from. The two addresses may be the same, but are prompted for separately, so that the trace display may be started after code which is known to be working and where tracing is not required.

Note that if the addresses are different the processor still single-step traces from the very start; but the display being only when the trace start address is encountered. Up to that point, therefore, the program will run considerably faster as there is no display taking place, but it will not run at full speed.

**TM** — *transparent mode.* A host computer may be connected to Port B and used for storing programs on its storage medium and assembling them. This command makes a transparent connection between the terminal and host allowing the terminal to work the host directly.

Control-S, control-Q and <del> are not intercepted but passed on to the host. The only character not transferred is the terminator, normally control—T, unless altered by *ST*.

**WB** — *write bytes to a memory location.* The *MO* command works fine for altering memory but is inconvenient when you wish to talk to peripheral devices, such as the PI/T or a d-to-a converter. But *WB* allows bytes to be written to any address, odd or even. It does not advance the address neither does it read back the data to check that the data stored correctly. D-to-a converters, for instance, normally cannot be read, only written to: so checking would serve no purpose.

The command asks first for the address of the byte to be operated on, then waits on a new line for successive pairs of hex digits to be entered. Each byte is stored at the chosen address.

The command is exited by <cr> or <del>.

*To be continued*

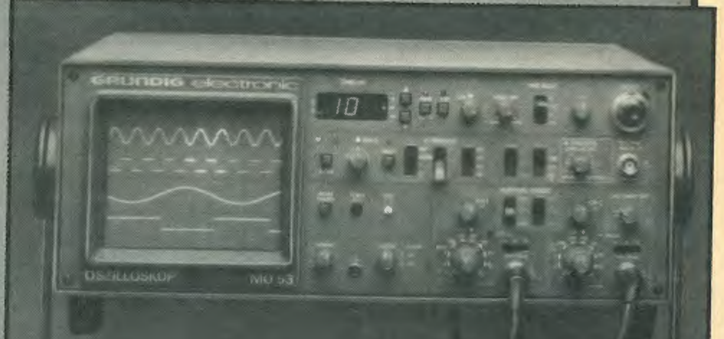
## GRUNDIG AND ELECTRONIC BROKERS

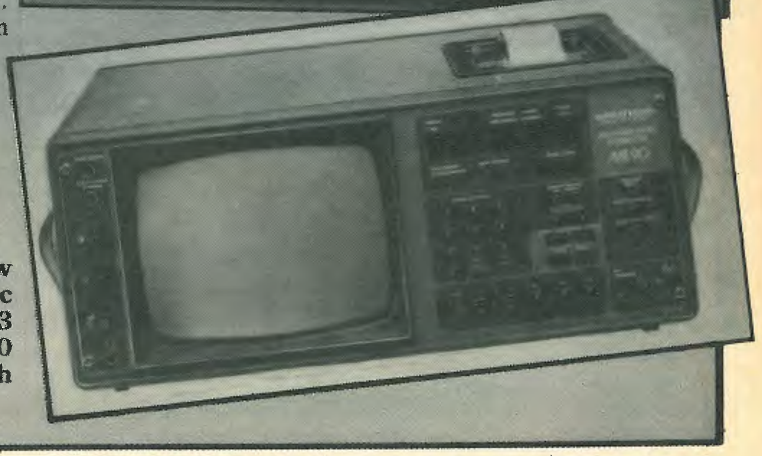
Grundig AG, well known in the UK as a manufacturer of domestic electronic equipment, also possesses a reputation for test and measurement instruments. In a recent move to obtain better penetration of the UK market for t. and m., the company has appointed Electronic Brokers as exclusive UK distributors of, initially, eight instruments from the Grundig range. Instruments covered by the agreement include oscilloscopes, video pattern generators and an automatic field-strength meter.

Top of the oscilloscope range is the M053, a 50 MHz dual-channel instrument with what Grundig call a 'user-friendly' time-base control, which automatically sets the time-base speed to suit the signal and displays the time-setting digitally. It offers all the usual X and Y deflection facilities of an instrument in this class, with the difference that the delayed B time-base is separately triggered.

ME90 is a microprocessor-controlled test receiver/field-strength meter covering from long-wave radio frequencies to 862 MHz television. The receiver can store 100 channel frequencies, which are push-button selected, and will carry out automatic level measurement with error correction. Frequency, channel and level are indicated digitally and printed out with time and date. By programming the print operation, the instrument can be left unattended.

Grundig and the Philips company co-operate closely, Philips having a 31.6% holding in the German company. The general manager and financial controllers are from Philips, but report to the Grundig board. Grundig is still in competition with Philips.





**Grundig instruments now handled by Electronic Brokers include the M053 oscilloscope and ME90 intelligent field-strength tester.**



# Rtty analyst

**by Ronald Alpiar**

## Using a computer to analyse radio teleprinter signals, automatically scanning, searching, detecting and translating messages

**Mr Alpiar was educated at Merchant Taylors' School, and Pembroke College, Cambridge, where he read mathematics and Ely Theological College, where he gained a diploma in theology and was ordained as a Anglican priest. There followed 25 years of work in research departments of universities and institutes in England and Switzerland, Mr Alpiar's interests being high-energy physics, reactor physics and computer applications. He retired early in 1980 to pursue his interests at leisure.**

Idly twiddling the tuning dial of your communications receiver readily demonstrates that the airwaves are dominated not by human speech but by a great variety of coded signals.

### Binary sequential codes

Apart from a single exception ('Piccolo') these signals can all be described as "binary serial codes" (b.s.cs) a pretentious phrase which is simply explained. It means that the signals consist of two elements only which may be on/off, or 0/1, or high/low, or short/long: and that these two elements are strung together in a continuous sequence. The nature of the two elements, and the ways they may be strung out are determined by coding rules: two typical such sets of rules (for r.t.t.y. and Morse) are illustrated in Figs. 1 and 2. In general, b.s.c. is such an effective means of communication that it is by no means limited to radio: telephone network messages are becoming increasingly b.s.c. in type, whether in the form of Prestel or many other systems.

Returning to radio, most b.s.cs encountered are some form of r.t.t.y, closely followed in popularity by high-speed Morse and the 'TOR' family of codes. Indeed the prevalence of r.t.t.y. has triggered a surge of amateur interests, the ready availability of r.t.t.y. decoder units and computer software to translate and display signals visually, but there is a snag!

The very efficiency of b.s.c. has spawned not only many types of code, but also a bewildering variety within each type — and this is especially true of r.t.t.y. Nor does the tale end here: further variations are found even within a variety — arising from the fact that transmission media and equipment distort or even violate the strict rules of coding. Some system of classification is needed to tidy the subject up: here a biological analogy can be of help. Just as living creatures are classified by genus, species and varieties, so too can b.s.cs.

The major groups of codes (r.t.t.y. Morse, AMTOR etc.) can be thought of as genera. Within each genus, many different species are to be found — Fig. 3 shows some of the species of r.t.t.y. Again, within each species, we can observe varieties — of which Fig. 4 provides some examples.

At first hearing it can be very hard to distinguish one genus from another (let alone identify the species and variety) — though long practice can help. Computer software designed for one genus will often display messages, even when fed with another: messages which are, needless to say, completely spurious. It is as if one were to attempt to translate an Arabic text by resorting to the rules of Chinese grammar! The result is much time fruitlessly wasted in trying to make sense of 'foreign' genera, or in stepping through all possible permutations of species, until something of significance appears — which may never transpire if the message is encrypted! Not only is this a horrible waste of time, but it is a formidable obstacle to programmed search operations which the alliance between home computers and amateur radio is making increasingly practical (see *Practical Wireless*, August/September, 1985).

What is clearly needed is a method of analysing any b.s.c., and supplying the user with precise information as to genus, species and variety and also maybe type of message content. Though this may appear a tall order, something very close to it may be achieved by exploiting the technique of spectral analysis. How this technique is able to identify true r.t.t.y., and also sort out its species and variety is the subject of the present article. However, the selfsame technique can be applied to any b.s.c. — and is by no means limited only to radio signals — enabling many other exotic fauna of the communications jungle to be detected, identified, classified, and in some cases even deciphered.

**Fig. 1 Coding rules for Morse**

1. There are two elements — signal and space (or no-signal).
2. There are two types of signal, the dot and the dash.
3. All dots are of exactly the same duration.
4. The length of the dash is exactly three dots.
5. Characters consist of sequences of up to six signals, as laid down in the Morse Code table.
6. Between each signal within a character, a space (or no-signal) equal to the length of a dot is inserted.
7. A space equal in length to three dots is inserted between characters.
8. Words consist of sequences of characters, as laid down in natural or formal languages.
9. A space equal in length to seven dots is interposed between words.

**Fig. 2 Coding rules for r.t.t.y.**

1. There are two elements — the mark and the space
2. All spaces are of the same length or duration
3. There are two types of mark, lasting exactly 1 or 1.5 times the length of a space
4. A character consists of a sequence of exactly five elements strung together, as laid down in the Baudot Table or elsewhere.
5. Within any character the length of the mark is exactly the length of the space.
6. A space precedes the five elements of each character
7. A 1.5-length mark follows the five elements of each character: this is the End-of-Character signal – EoC.

**Fig. 3 Species of r.t.t.y.**

| | |
|---|---|
| *Frequency shift,* | 170, 425, 850, 900Hz or non-standard |
| *Speed* | 45.45, 50, 75, 100 baud or non-standard |
| *Polarity* | normal, reverse |

**Fig. 4 Variations within species of r.t.t.y.**

| | |
|---|---|
| *Bias distortion* | mark and space of slightly unequal length |
| *EoC variation* | End-of-Character mark length not exactly 1.5 times space length |
| *Scatter* | Lengths of marks and spaces scattered around correct lengths |

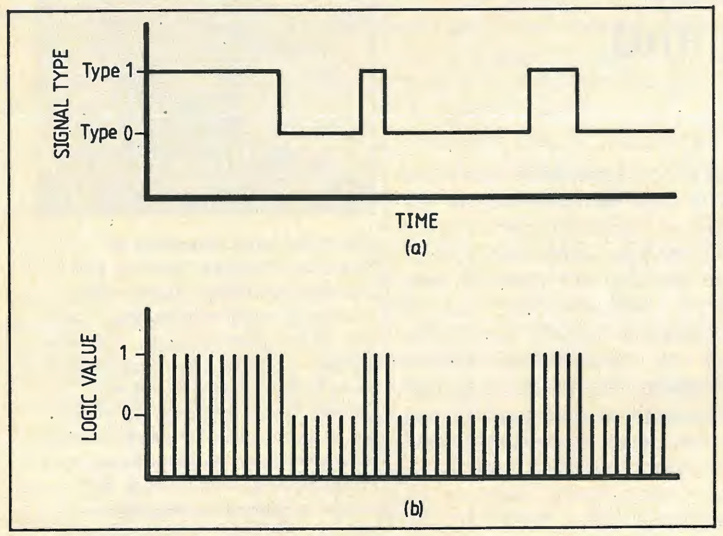



**Fig. 5 Signal type against time at (a), while (b) shows the same as 'seen' by a computer.**

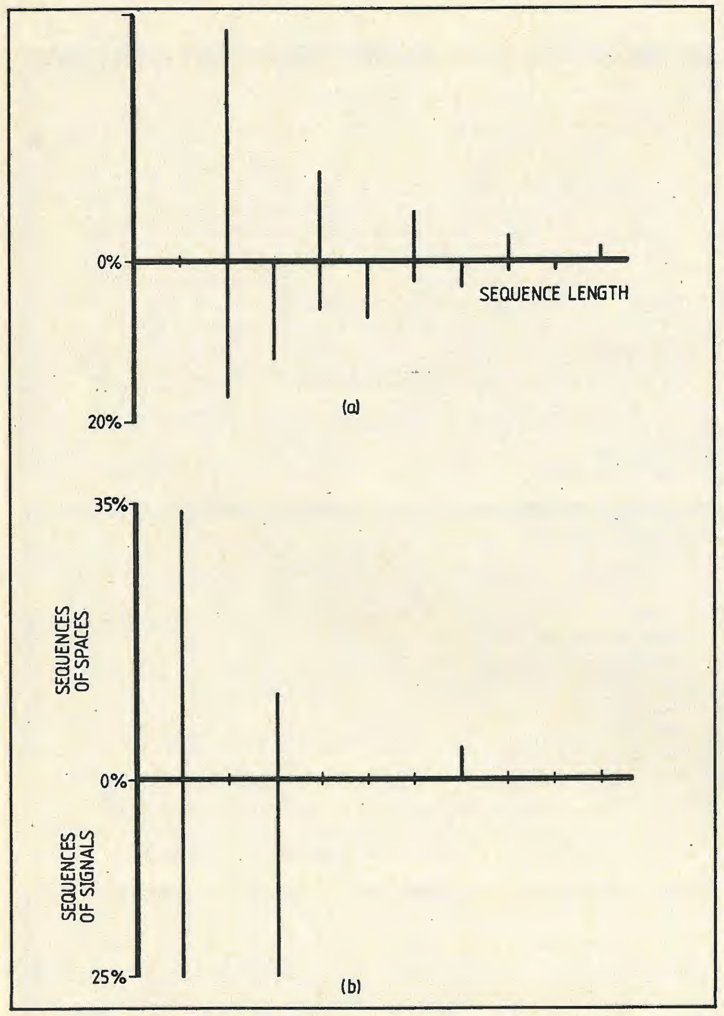



**Fig. 6 At (a), the sequence-length spectrum of random r.t.t.y., with that of random Morse at (b).**

## Sequence-length spectra

Since a b.s.c. contains only two types of signal strung together, we can plot signal type against time as in Fig. 5(a). In practice, a demodulator or other hardware is interposed to differentiate between the two types of signal, and to translate them into low or high voltage levels. The computer in turn "sees" these as 0 or 1 logic levels. Moreover, being a digital device, the computer is unable to sample signal levels continuously, but only at finite regular intervals. The result, as far as the computer is concerned, is shown in Fig. 5(b).

We define a sequence as a period of time over which the signal type is constant, and its length is simply that time period. As seen by the computer all sequence lengths are integers (related to time by the sampling rate), and there are two types of sequence corresponding to the two types of signal.

Individual sequence lengths are determined by coding rules and the particular character being transmitted. But something very interesting happens if we take a large sample, and plot percentages of occurrences of sequences of a given length against that length. It turns out that the resulting spectrum is practically independent of the message being transmitted, but highly characteristic of the b.s.c. genus, species and variety. It is almost as if each b.s.c. had its own uniquely identifiable fingerprint no matter what message it was carrying!

Figures 6(a) and 6(b) illustrate the characteristic spectra of r.t.t.y. and Morse. The two types of sequence are distinguished by being plotted above and below the horizontal sequence-length axis respectively. They were obtained by generating messages consisting of random sequences of characters, and then analysing the resulting sequence lengths. But precisely what features of, say, Fig. 6(a) characterise it as an r.t.t.y. spectrum — and why?

To understand the answers, it is helpful first to define the idea of a b.s.c. time unit — t.u. for short. In the case of r.t.t.y. this is simply the length of time occupied by a single space (or mark — being of the same length). Of course, this varies according to the transmission speed. At the slowest speed of 45.45 baud, 1 t.u. = 22 milliseconds: whilst at the normally highest speed of 100 baud, 1 t.u. is only 13.4 ms.

According to the r.t.t.y. coding rules, 1,2,3,4 or 5 spaces can be strung together — no other space lengths can legally occur. You can't have six spaces since this would imply one start space followed by five data spaces — and five spaces is not a legal character in r.t.t.y. Thus the sequence length spectrum will contain spectral lines for sequences of spaces at 1,2,3,4 and 5 t.us — 5 and only 5 space lines.

On the other hand marks can be strung together 1,2,3 or 4 at a time (5 marks would have to be followed by the 1.5 t.u. EoC signal). If a sequence of marks is followed by a stop we also get mark lengths of 1.5, 2.5 . . . 6.5 t.us. Altogether this gives us 10 and only 10 mark lines in the sequence length spectrum. Of course, if the polarity of the r.t.t.y. transmission is reverse polarity, we simply interchange mark and space in the above analysis.

On the other hand, the sequence length spectrum for Morse (Fig. 6(b) has lines at only 1,3 and 7 t.us: the explanation of this, in terms of the Morse coding tules, is left as an exercise for the reader!

So far, we have considered only the positions of the spectral lines: what about their heights — i.e. the relative percentages of sequences of various t.u. lengths? Normally this is a matter of lesser consequence, since it is the spacing of the lines which characterise the r.t.t.y. speed and polarity. However, there is a snag. Random messages give spectral line heights as in Fig. 6(a) — and messages in ordinary language give line heights which are scarcely distinguishable from random messages. However, messages consisting of a strictly limited set of characters will produce severe distortions of line height. Consider for example a message restricted to the two characters R and Y (either as RYRYRY . . . or in a random sequence). The codes for R and Y are 01010 and 10101 respectively. This gives only the following spectral lines:

space: 1, 2 t.us

mark: 1, 1.5, 2.5 t.us

Thus, restricted messages can distort the heights of spectral lines even to the extent of eliminating them. When testing a sequence-length spectrum, it is therefore essential to take into account the possibility that some of the normally expected spectral lines may be absent. Of course, this is most severe in the case of what one might call pathological messages. But even a transmission restricted to digits only will leave its imprint on the sequence-length spectrum: the lines at 4.5, 5.5 and 6.5 t.us disappear, and those at 3 t.us characteristically inverted in their mark and space frequencies.

To summarize, the positions of lines in the sequence-length spectrum provide evidence for genuine r.t.t.y., its speed and polarity, whilst the heights of lines supply clues as to the nature of the message.

## Real spectra

So far, we have considered only an ideal world, in which r.t.t.y. coding rules are strictly observed, and no transmission medium distortion mars the message. In the real world, alas, these assumptions are very far from true. What kind of distortion of the ideal sequence-length spectra can we expect to observe in practice?

The commonest r.t.t.y. variations contain bias distortion, and EoC (end-of-character) variation (see Fig. 4). Typically the mark may be up to 20% longer than the space, and the EoC may vary from 1.25 to 1.75 space length. The effects of these are to shift spectral lines slightly away from their correct positions. Further, individual marks and spaces may vary slightly in length, and transmission speeds may 'wow' or 'flutter'. The result is to smear sharp spectral lines into a cluster of peaks and troughs. The presence of noise will cut sequences up into smaller fragments: the characteristic debris of pathologically short sequences will be deposited as 'grass mowings' at the extreme left of the spectrum. Finally discrete sampling resaults in sequence length measurements whose significance depends on the sampling rate. The upshot of all this is that instead of the clean lines of Fig. 6(a), we are more likely to encounter something like Fig. 7.

If the distortion is so severe as to produce ambiguity (e.g. inability to decide whether a received sequence is a mark or an EoC signal) then it will be difficult to interpret it correctly. However, short of this, and provided we take a sufficiently large sample, mathematical methods can usually detect underlying r.t.t.y. in even a shockingly dirty spectrum, identifying the species, and giving useful information about the variety. The latter is not without value, since r.t.t.y. abnormality is often characteristic of the type of transmitting equipment, and the care exercised in its adjustment. In some cases one can even identify stations by their tell-tale peccadillos — rather like the modus operandi of a criminal! In all his experience the author has only come across one station transmitting r.t.t.y. as perfect as his analysis could detect (from Warsaw at 13.793 MHz).

## Programming methods

By exploiting the characteristics of r.t.t.y. described above, and in conjunction with computer-controlled receiver frequency tuning (see author's articles *Practical Wireless* August/September, 1985) we can set up a completely automatic system of scanning frequencies for the presence of r.t.t.y. and issuing reports on frequency, r.t.t.y. species/variation, time of day, sample of received text, and even some simple textual analysis. Given an on-line printer the program can proceed automatically and unattended. At the end of a session all the user need do is to glance at the printed reports, and single out interesting transmissions deserving further investigation.

Rather than listing and describing the author's program line-by-line, it may be more helpful to explain the mathematical and programming principles involved. Armed with these any reasonably competent programmer should have little difficulty (but much fun!) in writing his own program. The computer should at least be capable of receiving the t.t.l. output signal levels from the r.t.t.y. decoder into a user port: this will enable reports to be issued on the basis of manual tuning. In order to enable automatic tuning the computer should have an additional analogue input port.

The overall flow diagram of the r.t.t.y. Analyst is shown in Fig. 8, and consists of Blocks 0-8, as explained in turn below.

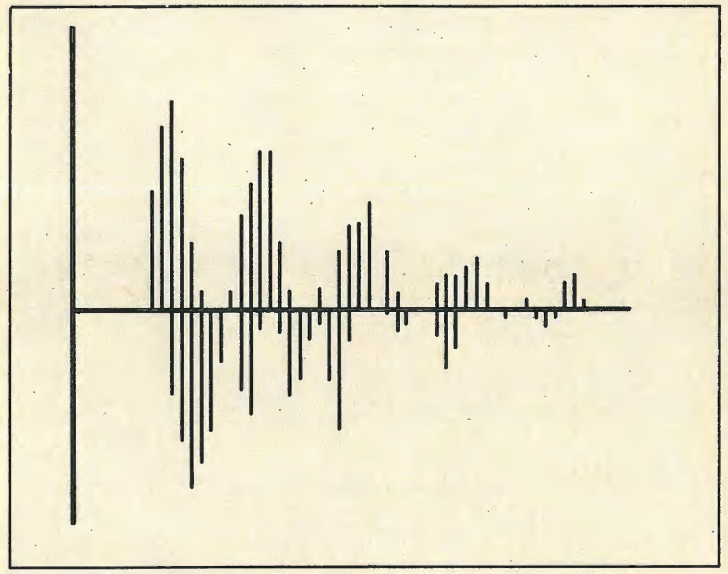
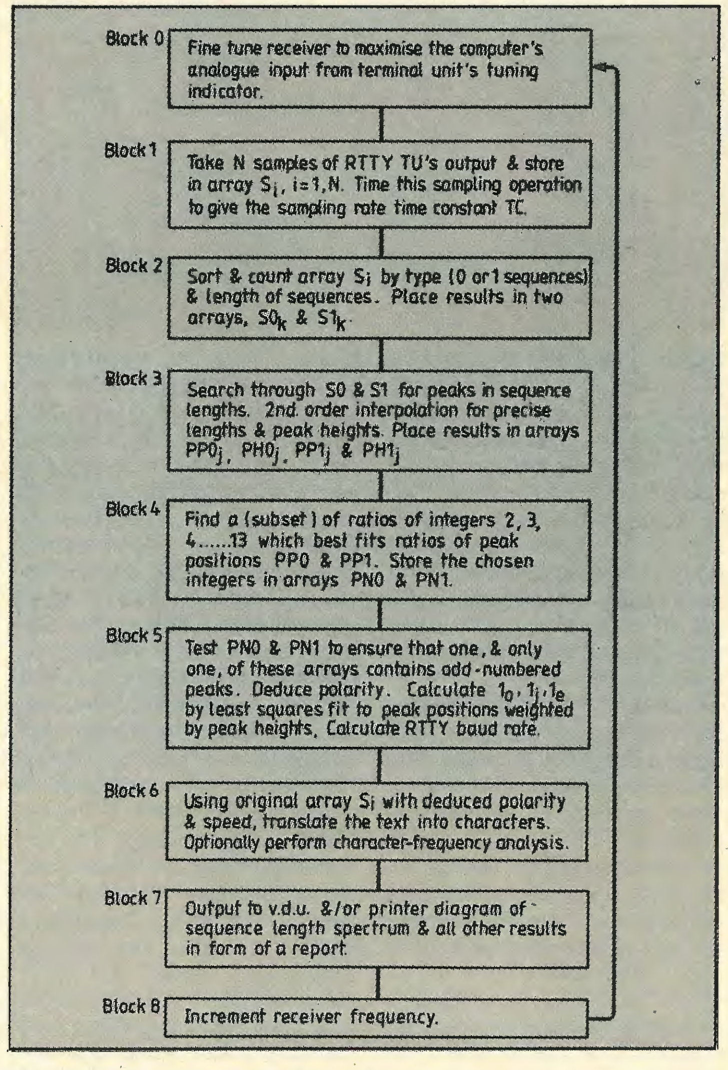


**Fig. 7 Sequence-length spectrum in practice, when signal distorted by transmission medium.**




**Flow diagram of r.t.t.y. analyst.**

**Fig. 9 Reports on good (a) and bad (b) examples of received r.t.t.y.**

Polarity Normal
Based on 4 Space peaks and 6 Mark peaks

| TYPE | SAMPLES | MSECS | BAUD |
|---|---|---|---|
| Space | 13.3 | 20.0 | 50.0 |
| Mark | 13.3 | 19.9 | 50.3 |
| EoC | 20.0 | 30.0 | 50.0 |

Bias Error = 0.4%  EoC Error = 0.8%

| TYPE-n | SAMPLES | HT% | TUs | MSEC | ERR% |
|---|---|---|---|---|---|
| Sp −0 | 13.4 | 25.8 | 1.0 | 20.0 | 0.3 |
| Sp −1 | 26.9 | 19.2 | 2.0 | 40.3 | 0.9 |
| Sp −2 | 39.9 | 10.0 | 3.0 | 59.9 | −0.0 |
| Sp −3 | 53.0 | 9.0 | 4.0 | 79.5 | −0.5 |
| Mk −0 | 13.3 | 20.9 | 1.0 | 19.9 | 0.0 |
| Mk −1 | 20.0 | 27.0 | 1.5 | 30.0 | 0.1 |
| Mk −2 | 26.9 | 7.0 | 2.0 | 40.3 | 1.4 |
| Mk −3 | 33.1 | 8.0 | 2.5 | 49.6 | −0.6 |
| Mk −4 | 39.1 | 3.0 | 3.0 | 58.6 | −1.8 |
| Mk −5 | 46.9 | 3.0 | 3.5 | 70.3 | 0.8 |

Text Reads:—
zzELE UM 15 PROZENT ZU SENKEN, BEREITS ERFUELL

Polarity Normal
Based on 4 Space peaks and 5 Mark peaks

| TYPE | SAMPLES | MSECS | BAUD |
|---|---|---|---|
| Space | 12.0 | 17.9 | 55.7 |
| Mark | 15.2 | 22.7 | 44.0 |
| EoC | 21.9 | 32.8 | 45.7 |

Bias Error = 26.7%  EoC Error = −5.8%

| TYPE-n | SAMPLES | HT% | TUs | MSEC | ERR% |
|---|---|---|---|---|---|
| Sp −0 | 11.8 | 22.7 | 1.0 | 17.6 | −1.5 |
| Sp −1 | 24.1 | 16.2 | 2.0 | 36.2 | 0.9 |
| Sp −2 | 37.8 | 10.2 | 3.0 | 56.7 | 5.1 |
| Sp −3 | 51.1 | 5.0 | 4.5 | 76.5 | −5.4 |
| Mk −0 | 15.3 | 17.1 | 1.0 | 23.0 | 1.2 |
| Mk −1 | 22.1 | 20.1 | 1.5 | 33.1 | 1.0 |
| Mk −2 | 29.0 | 8.0 | 2.0 | 43.5 | −4.6 |
| Mk −3 | 35.9 | 4.0 | 2.5 | 53.8 | −3.1 |
| Mk −4 | 48.0 | 3.0 | 3.0 | 72.0 | 5.2 |

Text Reads:—
zzURE AxGAINST xPRETxORIAx'xS INTERNAL AND ExXTERNAL

**Block 0 (tuning).** It is assumed that the r.t.t.y. terminal unit contains some sort of indication (meter or lamp) to indicate correct tuning on the mark and space frequencies, and a knob to adjust the frequency shift between the two. The usual method of manual tuning is to tune the receiver to maximize one of the two indicators, and then to tune the terminal unit to maximize the other.

However, it is difficult to perform the second of these tunings under full computer control: fortunately in the case of most terminal units it is unnecessary. That is, good r.t.t.y. can be decoded by tuning the receiver only, and forgetting about the space-mark frequency shift. The author uses a terminal unit built from a kit (Maplin's TU 1000) — which is eminently satisfactory in this respect. One merely tunes the receiver to maximize the reading of the right-hand meter, the terminal unit's frequency shift control being left permanently in the 1000Hz shift position — i.e. beyond the range of any shift normally encountered.

To fine tune automatically, some sort of feedback from the terminal unit is needed. A simple hardware link from the terminal unit's tuning indicator to the computer analogue port will provide the necessary feedback. Software monitors this output level whilst fine tuning the receiver's frequency.

**Block 1 (sampling).** The terminal unit's output, low or high, is recognised as a 0 or 1 t.t.l. logical level at the computer's input user port. This port is sampled at regular fine intervals, and the results are stored as a continuous sequence of 0s and 1s in the array $S_1$. The author's program gathers 5000 samples in a simple Basic loop — resort to machine code is not necessary. The whole loop is timed internally, and its duration, divided by N = 5000 gives the sampling rate TC. On the BBC-B micro this will usually be around TC = 1.5ms. This sampling rate is quite fast enough to allow analysis of r.t.t.y. speeds well over the maximum normally encountered 100 baud.

**Block 2 (sort and count).** This loop distinguishes between sequences of 0s and sequences of 1s in the array $S_i$, and counts the length (i.e. the number of consecutive samples) in each sequence. The resulting arrays $S0_j$ and $S1_j$ are formed, defined as:

$S0_j$ the number of sequences of 0s in the array $S_i$ of length j units.

$S1_j$ similarly for sequences of 1s.

The subscript j commonly ranges from about 5 to 100 units depending on r.t.t.y. speed and upon the number of marks or spaces strung together.

**Block 3 (locate the peaks).** Each of the arrays S0 and S1 is scanned for the presence of peaks in sequence lengths. Each time such a peak is detected (middle member of set of three sequence lengths occurring more often than either of its two neighbours) the triplet is fitted to a parabola to give the precise position and height of the peak. These results are stored in 4 arrays PP0, PH0, PP1, PH1 as follows:

$PP0_j$ is the calculated position (i.e. sequence length) of the j-th peak of sequences of 0s.

$PH0_j$ is the height of this j-th peak (i.e. the number of sequences of length $PP0_j$.

$PP1_j$ $PH1_j$ are similarly defined for sequence of 1s

As a bonus we may also store the width of the parabola calculated to fit the peak. Although this width plays no further part in the analysis, it provides evidence of the amount of scatter in the received r.t.t.y.

**Block 4 (fit to ratios of integers).** In good r.t.t.y., sequence lengths should be close to if not exactly 1, 1.5, 2, 2.5 . . . 6.5 time units in length. In other words the ratios of sequence lengths should be close to the ratios of the integers 2,3,4, . . . 13. But as explained earlier, not all these sequence lengths need be present in a given r.t.t.y. sample. This block makes a selection of those integers 2-13 whose ratios best fit the ratios of sequence lengths PP0 and PP1. This selection is further constrained by the requirement that the r.t.t.y. speed lie within acceptable limits — say 40-120 band. An example with two peaks only will make this clearer: Given the lengths of the first two peaks of zero sequence lengths $PP0_1$ and $PP0_2$ we have to select two integers, h and k, in the range 2-13 which minimize the expression

$$ABS(PP0_2/PP0_1 - h/k)$$

subject to the constraints that both $PP0_2/h$ and $PP0_1/k$ lie within certain fixed lower and upper limits. These limits are obtained by simply dividing the t.us for the fastest and slowest acceptable r.t.t.y.s respectively, by the sampling time constant TC.

Granted that this is all rather cumbersome to explain in words, it is nevertheless extremely simple to program! For each peak in PP0 or PP1, the corresponding 2-13 integer is stored in arrays PN0 and PN1. Note that odd integers indicate a sequence consisting of data followed by an EoC.

**Block 5 (Calculate $l_0$, $l_1$ & $l_e$ by least squares.** All the analysts's most important calculations are performed in this block. The first stage is to deduce the polarity (normal or reversed) of the r.t.t.y. — if indeed the sample appears to conform to r.t.t.y. coding rules. The latter say that an EoC signal of 1.5 time units must be placed after the data signals of each character, and that this EoC is at mark level. We therefore scan the two arrays PN0 and PN1 for the presence of *odd* integers. If neither or both the arrays contain odd integers, this indicates a fundamental violation of r.t.t.y. rules — the sample must be in some other code. This leaves us the case of only one of the arrays PP0/PP1 containing odd integers. If it is the array PP1, then the r.t.t.y. polarity is normal; if PP0 then it is reversed.

The next task is to calculate the length in time units of one space $-l_0$, of one mark $-l_1$, and of the EoC signal $-l_e$. This is done by least-squares fitting the sequence lengths PP0 and PP1 to appropriate time units. What we are looking for in the case, say, of $l_0$ is a value such that each $PP0_j$ is as close as possible to $PN0_j \times l_0$.

The difference between the actual and the calculated values of peak positions are squared, weighted by peak height, and added together. The result is the following function of $l_0$

$$M(l_0) = PH0_1 \times (PP0_1 - PN0_1 \times l_0/2)^2 + PH0_2 \times (PP0_2 - PN0_2 \times l_0/2)^2 \text{ etc.} + \ldots \text{(a term for each peak } PP0_i$$

The sigma character is conveniently used to make the expression more compact, thus

$$M(l) = \sum_j PH0_j \times (PH0_j - PN0_j \times l_0/2)^2$$

This expression must now be minimized with respect to $l_0$. Differentiating and gathering terms together we get a simple equation for $l_0$

$$\left\{\sum_j PH0_j \times PN0_j^2\right\} \times l_o = 2 \times \sum_j PH0_j \times PN0_j \times PP0_j$$

which gives $l_0$. The calculation of $l_1$ and $l_e$ is a little more complicated. The function to be minimized $M(l_1, l_e)$ is here a function of both unknowns at once. There are also two partial derivatives $\partial M/\partial l_1$ and $\partial M/\partial l_e$ to be set to zero. This gives us two simultaneous equations for $l_1$ and $l_e$.

The expression for M is

$$M(l_1, l_e) = \sum_{even} PH1_j \times (PP1_j - PN1_j \times l_1/2)^2 + \sum_{odd} PH1_j \times (PP1_j - (PN1_j - 1.5) \times l_1/2 - l_e)^2$$

Taking the partial derivatives, forming and solving the two simultaneous equations is then a matter of simple calculus and algebra.

Now, armed with the three $l_0$, $l_1$ and $l_e$ we can calculate bias error = $100 \times (l_1/l_0 - 1)$ %, and EoC error = $100 \times (l_e/l_1 - 1.5)$%. The r.t.t.y. time unit (duration of one space unit in milliseconds is just $l_0 \times TC$ (the time constant for sampling): from this the r.t.t.y. baud rate is easily deduced. We can also calculate, as a matter of interest, the percentage divergence of each PP0 and PP1 peak from its correct value, as the appropriate multiple of $l_0$ or $l_1$ or $l_1$ with EoC signal $l_e$.

This completes the bulk of the mathematics involved. Let me again assure the reader that when programmed it is very much less alarming than at first appears!

**Block 6 (translate sampled r.t.t.y.).** Using our calculated space, mark and EoC lengths $l_0$, $l_1$ and $l_e$ there is no problem scanning the original data stored in the array $S_i$: each time an EoC is encountered, the numerical value of the previous data is calculated to give the actual character position in a Baudot Table. The presence of letter-shift and figure-shift characters previously encountered determines which column of the table to use.

This all presupposes that the r.t.t.y. is of good quality. If not, things start to get a little hairy! The most likely cause of ambiguity is between a sequence of marks, and a sequence consisting of one fewer marks followed by an EoC. These sequence lengths differ by only half a t.u., as opposed to sequences of spaces whose lengths differ by a full t.u. Fortunately there is a way of resolving this difficulty which works well in most cases. Since the Baudot rules specify exactly 1 space followed by 5 data bits between EoCs, we can usually (not always) determine the true nature of a questionable sequence.

In the author's program such characters are printed in a contrasting colour so that a glance at the text shows how much second guessing was needed in order to translate it.

At this stage, the program has all the information required to perform a frequency analysis of the characters in the text, from which it could deduce the nature and even content of the message. It is easy to detect the difference between messages consisting of strings of 5-digit integers (frequently encountered) from normal texts. Call signs can be detected by recognition of the prompt sequence "DE": Western text can be distinguished from Arabic language messages. However we are here bordering on the giant topic of textual analysis and cryptography, and several further articles would be required to do justice to the subject. So here we must be content to note that both the information and the methods to perform a far more penetrating analysis of r.t.t.y. messages are to hand.

**Block 7 (print diagram and report).** All the findings of the previous blocks are here output: but with slight differences between v.d.u. screen output (where colour can be exploited) and printer hard copy (colour capability not commonly available).

Thus, on the v.d.u. the sequence-length spectrum is drawn with colour coding distinguishing 0 and 1 sequence lengths, whilst on the printer they are distinguished by being drawn above and below the horizontal axis respectively. Likewise the printer lacks the luxury of coloured table headings, and colour-coding sections of 'dubious' text. Typical results from the author's program are presented in Fig. 9. Although these examples are genuine as to content, their form has had to be somewhat modified to the limitations of print. Instead of colour, the letters (x) and (z) in translated text indicate recoverable and non-recoverable code errors respectively.

**Block 8 (increment frequency).** THis job can be done either manually, or under software computer control. In the latter case we could either step through a stored set of known r.t.t.y.-rich frequencies, or search continuously between assigned frequency limits. Bearing in mind the width of transmission r.t.t.y. frequency spectra there is little point in incremental steps smaller than 1kHz — especially as a further fine tuning operation will be performed in Block 0.

## Results

The results of two typical analyses are given in Fig 9. The (a) figures relate to an unusually good example of r.t.t.y., whilst the (b) results belong to an all-too-common bad example.

The reports proper (Figs 9(a) and (b)) consist of six items.

- Polarity (normal or reversed).
- The number of significant peaks of sequence lengths of space and mark types on which the subsequent analysis is based.
- For each of the unit space, mark and EoC signals the program prints the average number of samples, the duration in milliseconds, and the Baud rate, based on that type of signal.
- The bias and EoC errors.
- For each significant peak of space and mark sequence lengths the program prints out:—
  - i. The peak number (starting at zero)
  - ii. The average number of samples for that peak
  - iii. The percentage of sequences associated with that peak
  - iv. The nearest number of time units (t.u.s) to that peak
  - v. The duration of the sequence in milliseconds
  - vi. The percentage error in least-square-fitting peak positions to their nearest number of t.u.s.
- Translation of the sample into text. In this 'z' represents an unrecoverable error (almost inevitably at the start of a sample), whilst 'x' precedes a character whose value was deduced by error recovery.

# 01-208 1177 TECHNOMATIC LTD 01-208 1177

## BBC Computer & Econet Referral Centre

**BBC B Plus 1 with DFS £369(a) £409 (a)BBC Plus with 128K kit £415(a); BBC B Plus Econet (no DFS) £370(a); Model B+Econet £335(a); B+Econet+DFS £399(a); 1770 DFS Upgrade for Model B £43.50(d)**

**Acorn 2nd Processors: 6502: £169(a); Z80: £299(a)**

**TORCH UNICORN: Z80 Card: £275(a); Z80 Disc Pack: £525(a)**

TORCH Graduate G800/2 £699(a)

**META-ASSEMBLER.** Both an editor and Macro-Assembler. Meta can assemble most 65xx, 68xx, 6804, 6805/6305, 6809, 8048, 8080/8085, Z80, 1802 and more. (Free updates due very soon — 68000 series, 8088/8086, Z8000 etc.) Many advanced features including Macros, conditional assembly, Global/selective search etc. etc. Includes 16K Eprom, disc, function key card, and comprehensive manual. Please phone for comprehensive leaflet. **Meta-Assembler £126(c)**

We stock the full range of ACORN hardware and firmware and a very wide range of other peripherals for the BBC. For detailed specifications and pricing please send for our leaflet.

### PRINTERS

EPSON: RX80T £175(a); LX80 £210(a); FX80 £265(a); FX80+£299(a); NEW FX105+incl NLQ & IBM mode £459(a); JX80 4 colour printer £499(a); LQ1500 Printer £899(a).

TAXAN KAGA: KP810 80 Col NLQ £230(a); **KP910 156 Col NLQ £339(a); JUKI 6100 Daisy Wheel £299(a).**

BROTHER: HR15(P) Daisy Wheel £299(a); HR15LX (Serial) £365(a).

PLOTTERS

**Epson H180:** A4 4 colour Plotter £345(a); Hitachi 672: A3 4 colour Plotter £475(a)

### ACCESSORIES

We hold a wide range of printer attachments (sheet feeders, tractor feeds etc) in stock. Serial, parallel, IEEE and other interfaces also available. Ribbons available for all above printers. Pens with a variety of tips and colours also available. Please phone for details and prices.

**Plain Fanfold Paper with extra fine perforation (Clean Edge):**
2000 sheets 9.5" × 11" £13(b) 2000 sheets 14.5" × 11" £18.50(b)
Labels per 1000s: Single Row 3½" × 1 7/16" £5.25(d) Triple Row 2-7/16" × 1 7/16" £5.00(d)

### MODEMS

**BUZZ BOX**

This pocket sized BT approved modem complies with V21 300/300 baud and provides an ideal solution for communications between users, with mainframe computers and bulletin boards. Suitable for use with Open University computer. Battery/mains powered.

**BUZZ BOX £55(c) mains Adaptor £10(d) BBC Data Lead £8(d)**

**MIRACLE WS 2000**

The world standard BT approved modem covering all standard CCITT and BELL (outside UK only) standards upto 1200 baud. Allows communication with virtually any computer system in the world. Expandability to Auto Dial and Auto Answer with full software control enhance the considerable features already provided on the modem. Mains powered. **WS 2000 £129 (c) Auto Dial Board/Auto Answer Board (awaiting BABT approval) £30 (d) Software Control Kit £10 (d)**

**NEW WS-3000 RANGE** — the new professional series. All are intelligent and 'Hayes' compatible, allowing simply 'English' commands to control its many features. All models feature Auto-Dial with 10 number memory, Auto-Answer, Speed Buffering, printer port, data security option etc. All models are factory upgradeable.

**WS3000 V2123** (V21 & V23 + Bell) **£295 (a)**
**WS3000 V22** (as above plus 1200 baud full duplex) **£495 (a)**
**WS3000 V22bis** (as above plus 2400 baud full duplex) **£650 (a)**
The WS3000 range all have BT approval.

**SOFTY II**

This low cost intelligent eprom programmer can program 2716, 2516, 2532, 2732, and with an adaptor, 2564 and 2764. Displays 512 byte page on TV — has a serial and parallel I/O routines. Can be used as an emulator, cassette interface.
Softy II ............ £195.00(b)
Adaptor for 2764/2564 ............ £25.00

**SPECIAL OFFER**
**2764-25 £2:00(d); 27128-25 £3:00(d); 6264 LP-15 £4:00(d);**

ACORN IEEE INTERFACE £278(a) | INDUSTRIAL PROGRAMMER EP8000 £695 (a)

### DISC DRIVES

TECHNOMATIC drives are fitted with high quality slimline mechanisms and are available with or without integral mains power supply. The high dual drive power supplies are switch mode type and are generously rated. All drives with integral power supply are fitted with a mains indicator.
All drives are supplied with all the necessary cables, manual and a formatting disc. All drives are capable of operating in single or double density modes.

| Single Drives: | Stacked Versions: |
|---|---|
| 1×100K 40T SS: TS100 £69(b) | PD200 2×100K 40T SS £195 (a) |
| PS100 with psu £89 (b) | PD800 2×400K 40/80T DS £199(a) |
| 1×400K 40/80T DS: TS400 £99 | 3.5" Drives |
| (b) PS400 with psu £120 | TS35 1×400K 80T DS £99 |
| Dual Drives: (with integral psu) | (b) TD35 2×400K 80T DS £172 (b) |

### 3M FLOPPY DISCS

Industry Standard floppy discs with a lifetime guarantee Discs in packs of 10.

| 5¼" DISCS | | | | 3½" DISCS | |
|---|---|---|---|---|---|
| 40 T SS DD | £13(d) | 40 T DS DD | £18(d) | 80 T SS DD | £30(d) |
| 80 T SS DD | £22(d) | 80 T DS DD | £24(d) | 80 T DS DD | £38(d) |

### FLOPPICLENE DRIVEHEAD CLEANING KIT

FLOPPICLENE Disc Head Cleaning Kit with 28 disposable cleaning discs ensures continued optimum performance of the drives. £14.50 (b)

**DRIVE ACCESSORIES**

| | |
|---|---|
| Single Disc Cable £6 (d) | Dual Disc Cable £8.50 (d) |
| 10 Disc Library Case £1.80 (d) | 30 Disc Storage Box £6 (c) |
| 30/40 Disc Lockable Box £14 (c) | 100 Disc Lockable Box £16(c) |

### MONITORS

All 14" monitors now available in plastic or metal cases, please specify your requirement.

**14" RGB 1431 Std Res £185 (a); 1451 Med Res £225 (a); 1441 Hi Res £385 (a).**
**14" RGB with PAL & Audio 1431 AP Std Res £199 (a) 1451 AP Med Res £275 (a)**
Swivel Base for Plastic 14" Microvitecs £20 (c)
**20" RGB with PAL & Audio 2030CS Std Res £380 (a); 2040CS Hi Res £685 (a).**

**KAGA TAXAN 12" RGB**
VISION II Hi Res £225 (a); VISION III Plus £330 (a)
SUPERVISION III Plus £330 (a)
MITSUBISHI 14" RGB Med RES IBM & BBC Compatible £299 (a)

**MONOCHROME MONITORS:**
SANYO DM8112CX Hi Res 12" Green Screen £86 (a)
KAGA KX1201G Hi Res 12" Etched Green Screen £92 (a)
KAGA KX1203A Hi Res 12" Etched Amber screen £105 (a)
PHILIPS BM7502 12" Hi Res Green Screen £75 (a)
PHILIPS BM7522 12" Hi Res Amber Screen £79 (a)
BBC Leads RGB £5(d) Microvitec £3.50m (d) Monochrome £3.50 (d)

### UVERASERS

UV1T Eraser with built-in timer and mains indicator. Built-in safety interlock to avoid accidental exposure to the harmful UV rays. It can handle up to 5 eproms at a time with an average erasing time of about 20 mins. £59 + £2 p&p. UV1 as above but without the timer. £47 + £2 p&p. For Industrial Users, we offer UV140 & UV141 erasers with handling capacity of 14 eproms. UV141 has a built in timer. Both offer full built in safety features UV140 £69, UV141 £85, p&p £2.50.

### PRINTER BUFFER

The buffer offers a storage of 64K. Data from three computers can be loaded into the buffer which will continue accepting data until it is full. The buffer will automatically switch from one computer to next as soon as that computer has dumped all its data. The computer then is available for other uses. LED bar-graph indicates memory usage. Simple push button control provides. REPEAT, PAUSE and RESET functions. Integral power supply. £199 (a).
BBC Cable Set £30.

**Serial Test Cable**
Serial Cable switchable at both ends allowing pin options to be re-routed or linked at either end — making it possible to produce almost any cable configuration on site.
Available as M/M or M/F £24.75 (d)

**Serial Mini Patch Box**
Allows an easy method to reconfigure pin functions without rewiring the cable assay. Jumpers can be used and reused. £22 (d)

**Serial Mini Test**
Monitors RS232C and CCITT V24 Transmissions, indicating status with dual colour LEDs on 7 most significant lines. Connects in Line. £22.50 (d)

### CONNECTOR SYSTEMS

**I.D. CONNECTORS** (Speedblock Type)

| No of ways | Header Plug | Recep-tacle | Edge Conn. |
|---|---|---|---|
| 10 | 90p | 85p | 120p |
| 20 | 145p | 125p | 195p |
| 26 | 175p | 150p | 240p |
| 34 | 200p | 160p | 320p |
| 40 | 220p | 190p | 340p |
| 50 | 235p | 200p | 390p |

**D CONNECTORS**

| No of Ways | 9 | 15 | 25 | 37 |
|---|---|---|---|---|
| **MALE:** | | | | |
| Ang Pins | 120 | 180 | 230 | 350 |
| Solder | 60 | 85 | 125 | 170 |
| IDC | 175 | 275 | 325 | — |
| **FEMALE:** | | | | |
| St Pin | 100 | 140 | 210 | 380 |
| Ang Pins | 160 | 210 | 275 | 440 |
| Solder | 90 | 130 | 195 | 290 |
| IDC | 195 | 325 | 375 | — |
| St Hood | 90 | 95 | 100 | 120 |
| Screw Lock | 130 | 150 | 175 | — |

**EDGE CONNECTORS**

| | 0.1" | 0.156" |
|---|---|---|
| 2×6-way (commodore) | — | 300p |
| 2×10-way | 150p | — |
| 2×12-way (vic 20) | — | 350p |
| 2×18-way | — | 140p |
| 2×23-way (ZX81) | 175p | 220p |
| 2×25-way | 225p | 220p |
| 2×28-way (Spectrum) | 200p | — |
| 2×36-way | 250p | — |
| 1×43-way | 260p | — |
| 2×22-way | 190p | — |
| 2×43-way | 395p | — |
| 1×77-way | 400p | 500p |
| 2×50-way(S100conn) | 600p | — |

**AMPHENOL CONNECTORS**
36 way plug Centronics (solder) 500p (IDC) 475p
36 way skt Centronics (solder) 550p (IDC) 500p
24 way plug IEEE (solder) 475p (IDC) 475p
24 way skt IEEE (solder) 500p (IDC) 500p
**PCB Mtg Skt Ang Pin**
24 way 700p 36 way 750p

**RIBBON CABLE** (grey/metre)

| | | | |
|---|---|---|---|
| 10-way | 40p | 34-way | 160p |
| 16-way | 60p | 40-way | 180p |
| 20-way | 85p | 50-way | 200p |
| 26-way | 120p | 64-way | 280p |

**DIL HEADERS**

| | Solder | IDC |
|---|---|---|
| 14 pin | 40p | 100p |
| 16 pin | 50p | 110p |
| 18 pin | 60p | — |
| 20 pin | 75p | — |
| 24 pin | 100p | 150p |
| 28 pin | 160p | 200p |
| 40 pin | 200p | 225p |

**GENDER CHANGERS** 25 way D type
Male to Male ........ £10
Male to Female ........ £10
Female to Female ........ £10

**EURO CONNECTORS**

| DIN 41612 | Plug | Skt |
|---|---|---|
| 2×32 way St Pin | 230p | 275p |
| 2×32 way Ang Pin | 275p | 320p |
| 3×32 way St Pin | 260p | 300p |
| 3×32 way Ang Pin | 375p | 400p |
| IDC Skt A+B | | 400p |
| IDC Skt A+C | | 400p |

For 2×32 way please specify spacing (A+B, A+C).

**RS 232 JUMPERS** (25 way D)
24" Single end Male £5.00
24" Single end Female £5.25
24" Female Female £10.00
24" Male Male £9.50
24" Male Female £9.50

**ATTENTION**
All prices in this double page advertisement are subject to change without notice.
ALL PRICES EXCLUDE VAT
Please add carriage 50p unless indicated as follows: (a) £8 (b) £2.50 (c) £1.50 (d) £1.00

**TEXTOOL ZIF SOCKETS** 28-pin £9.00 24-pin £7.50 40-pin £12.00

**MISC CONNS**
21 pin Scart Connector 200p
8 pin Video Connector 200p

**DIL SWITCHES**
4-way 90p 6-way 105p
8-way 120p 10-way 150p

**TECHNOLINE VIEWDATA SYSTEM. TEL: 01-450 9764**
Using 'Prestel' type protocols. For information and orders — 24 hour service, 7 days a week



### 74 SERIES

| | |
|---|---|
| 7400 | 0.30 |
| 7401 | 0.30 |
| 7402 | 0.30 |
| 7403 | 0.30 |
| 7404 | 0.36 |
| 7405 | 0.30 |
| 7406 | 0.40 |
| 7407 | 0.40 |
| 7408 | 0.30 |
| 7409 | 0.30 |
| 7410 | 0.30 |
| 7411 | 0.30 |
| 7412 | 0.30 |
| 7413 | 0.50 |
| 7414 | 0.50 |
| 7416 | 0.36 |
| 7417 | 0.40 |
| 7420 | 0.30 |
| 7421 | 0.60 |
| 7422 | 0.36 |
| 7423 | 0.36 |
| 7425 | 0.40 |
| 7426 | 0.40 |
| 7427 | 0.40 |
| 7428 | 0.43 |
| 7430 | 0.30 |
| 7432 | 0.36 |
| 7433 | 0.40 |
| 7437 | 0.40 |
| 7438 | 0.40 |
| 7440 | 0.40 |
| 7441 | 0.90 |
| 7442A | 0.70 |
| 7443 | 1.00 |
| 7444 | 1.10 |
| 7445 | 1.00 |
| 7446A | 1.00 |
| 7447A | 1.00 |
| 7448 | 1.00 |
| 7450 | 0.36 |
| 7451 | 0.30 |
| 7453 | 0.36 |
| 7454 | 0.36 |
| 7460 | 0.36 |
| 7470 | 0.50 |
| 7472 | 0.45 |
| 7473 | 0.50 |
| 7474 | 0.50 |
| 7475 | 0.50 |
| 7476 | 0.50 |
| 7480 | 0.65 |
| 7481 | 1.80 |
| 7483A | 1.05 |
| 7484A | 1.25 |
| 7485 | 1.10 |
| 7486 | 0.42 |
| 7489 | 2.10 |
| 7490A | 0.55 |
| 7491 | 0.70 |
| 7492A | 0.70 |
| 7493A | 0.55 |
| 7494 | 1.10 |
| 7495A | 0.60 |
| 7496 | 0.80 |
| 7497 | 2.10 |
| 74100 | 1.90 |
| 74107 | 0.50 |
| 74109 | 0.75 |
| 74110 | 0.75 |
| 74111 | 0.55 |
| 74116 | 1.70 |
| 74118 | 1.10 |
| 74119 | 1.70 |
| 74120 | 1.00 |
| 74121 | 0.55 |
| 74122 | 0.70 |
| 74123 | 0.80 |
| 74125 | 0.65 |
| 74126 | 0.55 |
| 74128 | 0.55 |
| 74132 | 0.75 |
| 74136 | 0.70 |
| 74141 | 0.90 |
| 74142 | 2.50 |
| 74143 | 1.30 |
| 74144 | 2.70 |
| 74145 | 1.10 |
| 74147 | 1.70 |
| 74148 | 1.40 |
| 74150 | 1.75 |
| 74151A | 0.70 |
| 74153 | 0.80 |
| 74154 | 1.40 |
| 74155 | 0.80 |
| 74156 | 0.90 |
| 74157 | 0.80 |
| 74159 | 1.75 |
| 74160 | 1.10 |
| 74161 | 0.80 |
| 74162 | 1.10 |
| 74163 | 1.10 |
| 74164 | 1.20 |
| 74165 | 1.10 |
| 74166 | 1.40 |
| 74167 | 4.00 |
| 74170 | 2.00 |
| 74172 | 4.20 |
| 74173 | 1.40 |
| 74174 | 1.10 |
| 74175 | 1.05 |
| 74176 | 1.00 |
| 74178 | 1.50 |
| 74179 | 1.50 |
| 74180 | 1.00 |
| 74181 | 3.40 |
| 74182 | 1.40 |
| 74184 | 1.80 |
| 74185A | 1.80 |
| 74190 | 1.30 |
| 74191 | 1.30 |
| 74192 | 1.10 |
| 74193 | 1.15 |
| 74194 | 1.10 |
| 74195 | 0.80 |
| 74196 | 1.30 |
| 74197 | 1.10 |
| 74198 | 2.20 |
| 74199 | 2.20 |
| 74221 | 1.10 |
| 74251 | 1.00 |
| 74259 | 1.50 |
| 74265 | 0.80 |
| 74273 | 2.00 |
| 74276 | 1.40 |
| 74278 | 1.70 |
| 74279 | 0.90 |
| 74283 | 1.05 |
| 74285 | 3.20 |
| 74290 | 0.90 |
| 74293 | 0.90 |
| 74298 | 1.80 |
| 74351 | 2.00 |
| 74365A | 0.80 |
| 74366A | 0.80 |
| 74367A | 0.80 |
| 74376 | 1.60 |
| 74390 | 1.10 |
| 74393 | 1.20 |
| 74490 | 1.40 |

### 74LS SERIES

| | |
|---|---|
| 74LS00 | 0.24 |
| 74LS01 | 0.24 |
| 74LS02 | 0.24 |
| 74LS03 | 0.24 |
| 74LS04 | 0.24 |
| 74LS05 | 0.24 |
| 74LS08 | 0.24 |
| 74LS09 | 0.24 |
| 74LS10 | 0.24 |
| 74LS11 | 0.24 |
| 74LS12 | 0.24 |
| 74LS13 | 0.40 |
| 74LS14 | 0.50 |
| 74LS15 | 0.24 |
| 74LS20 | 0.24 |
| 74LS21 | 0.24 |
| 74LS22 | 0.24 |
| 74LS24 | 0.50 |
| 74LS26 | 0.26 |
| 74LS27 | 0.24 |
| 74LS28 | 0.24 |
| 74LS30 | 0.24 |
| 74LS31 | 0.24 |
| 74LS32 | 0.24 |
| 74LS33 | 0.24 |
| 74LS37 | 0.24 |
| 74LS38 | 0.24 |
| 74LS40 | 0.24 |
| 74LS42 | 0.50 |
| 74LS47 | 0.90 |
| 74LS48 | 0.90 |
| 74LS49 | 1.00 |
| 74LS51 | 0.24 |
| 74LS54 | 0.24 |
| 74LS55 | 0.24 |
| 74LS63 | 1.25 |
| 74LS73A | 0.30 |
| 74LS74A | 0.36 |
| 74LS75 | 0.45 |
| 74LS76A | 0.36 |
| 74LS83A | 0.70 |
| 74LS85 | 0.75 |
| 74LS86 | 0.35 |
| 74LS90 | 0.48 |
| 74LS91 | 0.90 |
| 74LS92 | 0.35 |
| 74LS93 | 0.54 |
| 74LS95B | 0.75 |
| 74LS96 | 0.90 |
| 74LS107 | 0.40 |
| 74LS109 | 0.40 |
| 74LS112 | 0.45 |
| 74LS113 | 0.45 |
| 74LS114 | 0.45 |
| 74LS122 | 0.70 |
| 74LS123 | 0.80 |
| 74LS125 | 0.50 |
| 74LS126 | 0.50 |
| 74LS132 | 0.65 |
| 74LS133 | 0.55 |
| 74LS136 | 0.45 |
| 74LS138 | 0.55 |
| 74LS139 | 0.55 |
| 74LS145 | 0.95 |
| 74LS147 | 1.75 |
| 74LS148 | 1.40 |
| 74LS151 | 0.65 |
| 74LS152 | 2.00 |
| 74LS153 | 0.65 |
| 74LS154 | 1.60 |
| 74LS155 | 0.65 |
| 74LS156 | 0.65 |
| 74LS157 | 0.50 |
| 74LS158 | 0.65 |
| 74LS160A | 0.65 |
| 74LS161A | 0.75 |
| 74LS162A | 0.75 |
| 74LS163A | 0.75 |
| 74LS164 | 0.75 |
| 74LS165A | 1.10 |
| 74LS166A | 1.50 |
| 74LS168 | 1.30 |
| 74LS169 | 1.00 |
| 74LS170 | 1.40 |
| 74LS173A | 1.00 |
| 74LS174 | 0.75 |
| 74LS175 | 0.75 |
| 74LS181 | 2.00 |
| 74LS183 | 1.90 |
| 74LS190 | 0.75 |
| 74LS191 | 0.75 |
| 74LS192 | 0.80 |
| 74LS194A | 0.75 |
| 74LS195A | 0.75 |
| 74LS196 | 0.80 |
| 74LS197 | 0.60 |
| 74LS221 | 0.90 |
| 74LS240 | 0.80 |
| 74LS241 | 0.80 |
| 74LS242 | 0.90 |
| 74LS243 | 0.90 |
| 74LS244 | 0.80 |
| 74LS245 | 1.10 |
| 74LS247 | 1.10 |
| 74LS248 | 1.10 |
| 74LS249 | 1.10 |
| 74LS251 | 0.75 |
| 74LS253 | 0.75 |
| 74LS256 | 0.90 |
| 74LS2457A | 0.70 |
| 74LS258A | 0.70 |
| 74LS259 | 1.20 |
| 74LS260 | 0.75 |
| 74LS266 | 0.60 |
| 74LS273 | 1.25 |
| 74LS279 | 0.70 |
| 74LS280 | 1.90 |
| 74LS283 | 0.80 |
| 74LS290 | 0.80 |
| 74LS292 | 9.00 |
| 74LS293 | 0.80 |
| 74LS295 | 1.40 |
| 74LS297 | 9.00 |
| 74LS298 | 1.00 |
| 74LS299 | 2.20 |
| 74LS321 | 3.70 |
| 74LS322A | 3.90 |
| 74LS323 | 3.00 |
| 74LS324 | 3.20 |
| 74LS348 | 2.00 |
| 74LS352 | 1.20 |
| 74LS353 | 1.20 |
| 74LS356 | 2.10 |
| 74LS363 | 1.80 |
| 74LS364 | 1.80 |
| 74LS365 | 0.50 |
| 74LS366 | 0.50 |
| 74LS367 | 0.52 |
| 74LS368 | 0.50 |
| 74LS373 | 0.90 |
| 74LS374 | 0.90 |
| 74LS375 | 0.75 |
| 74LS377 | 1.30 |
| 74LS378 | 0.95 |
| 74LS379 | 1.30 |
| 74LS381 | 4.50 |
| 74LS385 | 3.25 |
| 74LS390 | 0.80 |
| 74LS393 | 1.00 |
| 74LS395A | 1.00 |
| 74LS399 | 1.40 |
| 74LS445 | 1.80 |
| 74LS465 | 1.20 |
| 74LS467 | 1.20 |
| 74LS490 | 1.50 |
| 74LS540 | 1.00 |
| 74LS541 | 1.00 |
| 74LS608 | 7.00 |
| 74LS610 | 19.00 |
| 74LS612 | 19.00 |
| 74LS624 | 3.50 |
| 74LS626 | 2.25 |
| 74LS628 | 2.25 |
| 74LS629 | 1.25 |
| 74LS640 | 2.90 |
| 74LS640-1 | 3.00 |
| 74LS641 | 2.90 |
| 74LS641-1 | 3.00 |
| 74LS642 | 2.50 |
| 74LS642-1 | 3.00 |
| 74LS643 | 2.50 |
| 74LS643-1 | 3.00 |
| 74LS644 | 3.50 |
| 74LS645 | 2.00 |
| 74LS645-1 | 3.00 |
| 74LS668 | 0.90 |
| 74LS669 | 0.90 |
| 74LS670 | 1.70 |
| 74LS682 | 2.50 |
| 74LS683 | 3.00 |
| 74LS684 | 3.50 |
| 74LS687 | 3.50 |
| 74LS688 | 3.50 |
| 74LS783 | 21.00 |

### 74S SERIES

| | |
|---|---|
| 74S00 | 0.50 |
| 74S02 | 0.50 |
| 74S04 | 0.50 |
| 74S05 | 0.50 |
| 74S08 | 0.50 |
| 74S10 | 0.50 |
| 74S11 | 0.75 |
| 74S20 | 0.50 |
| 74S22 | 0.50 |
| 74S30 | 0.50 |
| 74S32 | 0.60 |
| 74S37 | 0.60 |
| 74S36 | 0.60 |
| 74S40 | 0.50 |
| 74S51 | 0.60 |
| 74S64 | 0.45 |
| 74S74 | 0.70 |
| 74S85 | 3.00 |
| 74S86 | 1.00 |
| 74S112 | 1.50 |
| 74S113 | 1.20 |
| 74S114 | 1.20 |
| 74S124 | 3.00 |
| 74S132 | 1.00 |
| 74S133 | 0.60 |
| 74S138 | 1.80 |
| 74S139 | 1.80 |
| 74S140 | 1.00 |
| 74S151 | 1.50 |
| 74S153 | 1.50 |
| 74S157 | 2.00 |
| 74S158 | 2.00 |
| 74S163 | 3.00 |
| 74S169 | 5.50 |
| 74S174 | 3.00 |
| 74S175 | 3.20 |
| 74S188 | 1.80 |
| 74S189 | 1.80 |
| 74S194 | 3.00 |
| 74S195 | 3.00 |
| 74S196 | 3.50 |
| 74S200 | 4.50 |
| 74S201 | 3.20 |
| 74S225 | 5.20 |
| 74S240 | 4.00 |
| 74S241 | 4.00 |
| 74S244 | 4.50 |
| 74S251 | 2.50 |
| 74S257 | 2.50 |
| 74S258 | 2.50 |
| 74S260 | 1.00 |
| 74S261 | 3.00 |
| 74S283 | 2.70 |
| 74S287 | 2.25 |
| 74S288 | 2.00 |
| 74S289 | 2.25 |
| 74S299 | 4.50 |
| 74S373 | 4.00 |
| 74S374 | 4.00 |
| 74S387 | 2.25 |

### 74C SERIES

| | |
|---|---|
| 74C00 | 0.70 |
| 74C04 | 0.50 |
| 74C08 | 0.70 |
| 74C10 | 0.70 |
| 74C14 | 0.50 |
| 74C20 | 0.70 |
| 74C30 | 0.70 |
| 74C32 | 1.00 |
| 74C42 | 1.50 |
| 74C48 | 1.90 |
| 74C73 | 1.00 |
| 74C74 | 1.00 |
| 74C76 | 1.00 |
| 74C83 | 2.00 |
| 74C85 | 2.25 |
| 74C86 | 1.00 |
| 74C89 | 5.00 |
| 74C90 | 1.90 |
| 74C93 | 1.50 |
| 74C95 | 1.50 |
| 74C107 | 1.00 |
| 74C150 | 5.00 |
| 74C151 | 2.00 |
| 74C157 | 2.50 |
| 74C160 | 1.80 |
| 74C161 | 1.80 |
| 74C162 | 1.80 |
| 74C163 | 1.80 |
| 74C164 | 1.80 |
| 74C173 | 1.60 |
| 74C174 | 1.50 |
| 74C175 | 1.50 |
| 74C192 | 1.50 |
| 74C193 | 1.50 |
| 74C194 | 1.50 |
| 74C195 | 1.50 |
| 74C200 | 9.50 |
| 74C221 | 2.50 |
| 74C240 | 2.25 |
| 74C244 | 2.25 |
| 74C373 | 2.25 |
| 74C374 | 2.25 |
| 74C901 | 0.80 |
| 74C902 | 1.20 |
| 74C911 | 9.00 |
| 74C912 | 9.00 |
| 74C915 | 1.80 |
| 74C922 | 4.50 |
| 74C923 | 5.00 |
| 74C925 | 6.50 |
| 74C926 | 7.50 |

### 74ALS SERIES

| | |
|---|---|
| 74ALS00 | 0.45 |
| 74ALS02 | 0.45 |
| 74ALS04 | 0.45 |
| 74ALS08 | 0.45 |
| 74ALS10 | 0.45 |
| 74ALS32 | 0.45 |
| 74ALS74 | 0.70 |
| 74ALS138 | 1.50 |
| 74ALS139 | 1.50 |
| 74ALS244 | 4.00 |
| 74ALS245 | 4.75 |
| 74ALS573 | 2.60 |
| 74ALS574 | 4.50 |
| 74ALS580 | 2.60 |

### 4000 SERIES

| | |
|---|---|
| 4000 | 0.20 |
| 4001 | 0.24 |
| 4002 | 0.25 |
| 4006 | 0.70 |
| 4007 | 0.25 |
| 4008 | 0.60 |
| 4009 | 0,45 |
| 4010 | 0.60 |
| 4011 | 0.24 |
| 4012 | 0.25 |
| 4013 | 0.36 |
| 4014 | 0.60 |
| 4015 | 0.70 |
| 4016 | 0.36 |
| 4017 | 0.55 |
| 4018 | 0.60 |
| 4019 | 0.60 |
| 4020 | 0.80 |
| 4021 | 0.60 |
| 4022 | 0.70 |
| 4023 | 0.30 |
| 4024 | 0.48 |
| 4025 | 0.24 |
| 4026 | 0.90 |
| 4027 | 0.40 |
| 4028 | 0.60 |
| 4029 | 0.75 |
| 4030 | 0.35 |
| 4031 | 1.25 |
| 4032 | 1.00 |
| 4033 | 1.25 |
| 4034 | 2.50 |
| 4035 | 0.70 |
| 4036 | 2.50 |
| 4037 | 1.10 |
| 4038 | 1.00 |
| 4040 | 0.60 |
| 4041 | 0.55 |
| 4042 | 0.50 |
| 4043 | 0.60 |
| 4044 | 0.60 |
| 4045 | 1.00 |
| 4046 | 0.60 |
| 4047 | 0.60 |
| 4048 | 0.55 |
| 4049 | 0.36 |
| 4050 | 0.35 |
| 4051 | 0.65 |
| 4052 | 0.60 |
| 4053 | 0.60 |
| 4054 | 0.80 |
| 4055 | 0.80 |
| 4056 | 0.85 |
| 4060 | 0.70 |
| 4063 | 0.85 |
| 4066 | 0.40 |
| 4067 | 2.30 |
| 4068 | 0.25 |
| 4069 | 0.24 |
| 4070 | 0.24 |
| 4071 | 0.24 |
| 4072 | 0.24 |
| 4073 | 0.24 |
| 4075 | 0.24 |
| 4076 | 0.65 |
| 4077 | 0.25 |
| 4078 | 0.25 |
| 4081 | 0.24 |
| 4082 | 0.25 |
| 4085 | 0.60 |
| 4086 | 0.75 |
| 4089 | 1.20 |
| 4093 | 0.35 |
| 4094 | 0.90 |
| 4095 | 0.95 |
| 4096 | 0.90 |
| 4097 | 2.70 |
| 4098 | 0.75 |
| 4099 | 0.99 |
| 4501 | 0.36 |
| 4502 | 0.55 |
| 4503 | 0.36 |
| 4504 | 0.95 |
| 4505 | 3.60 |
| 4506 | 0.90 |
| 4507 | 0.35 |
| 4508 | 1.20 |
| 4510 | 0.55 |
| 4511 | 0.55 |
| 4512 | 0.55 |
| 4513 | 1.50 |
| 4514 | 1.10 |
| 4515 | 1.10 |
| 4516 | 0.55 |
| 4517 | 2.20 |
| 4518 | 0.48 |
| 4519 | 0.32 |
| 4520 | 0.60 |
| 4521 | 1.15 |
| 4522 | 0.80 |
| 4526 | 0.70 |
| 4527 | 0.80 |
| 4528 | 0.65 |
| 4529 | 1.00 |
| 4530 | 0.75 |
| 4531 | 0.65 |
| 4534 | 3.80 |
| 4536 | 2.50 |
| 4538 | 0.75 |
| 4539 | 0.75 |
| 4541 | 0.90 |
| 4543 | 0.70 |
| 4551 | 1.00 |
| 4553 | 2.40 |
| 4555 | 0.36 |
| 4556 | 0.50 |
| 4557 | 2.40 |
| 4560 | 1.40 |
| 4566 | 1.40 |
| 4568 | 2.40 |
| 4569 | 1.70 |
| 4572 | 0.45 |
| 4583 | 0.90 |
| 4584 | 0.48 |
| 4585 | 0.60 |
| 4724 | 1.50 |
| 14411 | 7.50 |
| 14412 | 7.50 |
| 14416 | 3.00 |
| 14419 | 2.60 |
| 14490 | 4.20 |
| 14495 | 4.50 |
| 145000 | 6.50 |
| 14599 | 2.00 |
| 22100 | 3.50 |
| 22101 | 7.00 |
| 22102 | 7.00 |
| 40014 | 0.48 |
| 40085 | 1.20 |
| 40097 | 0.36 |
| 40098 | 0.40 |
| 40100 | 1.50 |
| 40101 | 1.25 |
| 40102 | 1.30 |
| 40103 | 2.00 |
| 40104 | 1.20 |
| 40105 | 1.50 |
| 40106 | 0.48 |
| 40107 | 0.55 |
| 40108 | 3.20 |
| 40109 | 0.80 |
| 40110 | 2.25 |
| 40114 | 2.25 |
| 40147 | 2.80 |
| 40163 | 1.00 |
| 40173 | 1.20 |
| 40174 | 1.00 |
| 40175 | 1.00 |
| 40192 | 1.00 |
| 40193 | 1.00 |
| 40194 | 1.00 |
| 40244 | 1.50 |
| 40245 | 1.50 |
| 40257 | 1.80 |
| 40373 | 1.80 |
| 40374 | 1.80 |
| 80C95 | 0.75 |
| 80C97 | 0.75 |
| 80C98 | 0.75 |

### LINEAR ICs

| | |
|---|---|
| AD7581 | 12.00 |
| ADC0808 | 11.90 |
| AM7910DC | 25.00 |
| AN-1-5050 | 1.00 |
| AY-3-1350 | 3.50 |
| AY-3-8910 | 4.90 |
| AY-3-8912 | 5.00 |
| CA3019A | 1.00 |
| CA3020 | 3.50 |
| CA3028A | 1.10 |
| CA3046 | 0.70 |
| CA3059 | 3.25 |
| CA3060 | 3.50 |
| CA3080E | 0.70 |
| CA3085 | 1.50 |
| CA3086 | 0.60 |
| CA3089E | 2.50 |
| CA3090AQ | 3.75 |
| CA3130E | 0.90 |
| CA3130T | 1.30 |
| CA3140E | 0.45 |
| CA3140T | 1.00 |
| CA3146 | 2.25 |
| CA3160E | 1.50 |
| CA3161E | 2.00 |
| CA3162E | 6.00 |
| CA3189E | 2.70 |
| CA3240E | 1.50 |
| CA3280G | 3.00 |
| D7002 | 6.00 |
| DAC1408-8 | 3.00 |
| DAC0800 | 3.00 |
| DAC0808 | 3.00 |
| DG308 | 3.00 |
| HA1366 | 1.90 |
| ICL7106 | 6.75 |
| ICL7611 | 0.95 |
| ICL7650 | 4.00 |
| ICL7660 | 2.50 |
| ICL8038 | 4.00 |
| ICM7216B | 22.00 |
| ICM7217 | 7.50 |
| ICM7555 | 0.90 |
| ICM7556 | 1.40 |
| LC7120 | 3.00 |
| LC7130 | 3.50 |
| LC7131 | 3.50 |
| LC7137 | 3.50 |
| LF347 | 1.20 |
| LF351 | 0.60 |
| LF353 | 0.90 |
| LF355 | 0.90 |
| LF356N | 1.10 |
| LF357 | 1.00 |
| LF398 | 4.00 |
| LM10CLH | 4.50 |
| LM301A | 0.30 |
| LM307 | 0.45 |
| LM308CN | 0.75 |
| LM310 | 2.25 |
| LM311 | 0.60 |
| LM318 | 1.50 |
| LM319 | 1.80 |
| LM324 | 0.45 |
| LM334Z | 1.15 |
| LM335Z | 1.30 |
| LM336 | 1.60 |
| LM339 | 0.40 |
| LM348 | 0.60 |
| LM358P | 0.50 |
| LM377 | 3.00 |
| LM380N-8 | 1.50 |
| LM380N | 1.50 |
| LM381AN | 1.70 |
| LM383 | 3.25 |
| LM384 | 2.20 |
| LM386N-1 | 1.00 |
| LM387 | 2.70 |
| LM389 | 1.89 |
| LM391 | 1.80 |
| LM392N | 1.10 |
| LM393 | 0.85 |
| LM394CH | 4.00 |
| LM709 | 0.35 |
| LM710 | 0.48 |
| LM711 | 1.00 |
| LM723 | 0.60 |
| LM725CN | 3.00 |
| LM733 | 0.65 |
| LM741 | 0.22 |
| LM7747 | 0.70 |
| LM748 | 0.30 |
| LM1011 | 4.80 |
| LM1014 | 1.50 |
| LM1801 | 3.00 |
| LM1830 | 2.50 |
| LM1871 | 3.00 |
| LM1872 | 3.00 |
| LM1886 | 6.00 |
| LM1889 | 4.50 |
| LM2917 | 3.00 |
| LM3302 | 0.90 |
| LM3900 | 0.80 |
| LM3909 | 1.00 |
| LM3911 | 1.80 |
| LM3914 | 3.50 |
| LM3915 | 3.40 |
| LM3916 | 3.40 |
| LM13600 | 1.50 |
| M51513L | 2.30 |
| M51516L | 4.50 |
| MB3712 | 2.00 |
| MC1310P | 1.50 |
| 1413 | 0.75 |
| MC1458 | 0.45 |
| MC1495 | 3.00 |
| MC1496 | 0.70 |
| MC3340P | 2.00 |
| MC3401 | 0.70 |
| MC3403 | 0.65 |
| MF10CN | 4.10 |
| MK50240 | 9.00 |
| MK50398 | 11.00 |
| ML902 | 5.00 |
| ML922 | 4.00 |
| MM6221A | 3.00 |
| NE529 | 2.20 |
| NE531 | 1.20 |
| NE544 | 1.90 |
| NE555 | 0.22 |
| NE556 | 0.60 |
| NE564 | 4.00 |
| NE565 | 1.20 |
| NE566 | 1.50 |
| NE567 | 1.25 |
| NE570 | 4.00 |
| NE571 | 3.00 |
| NE592 | 0.90 |
| NE5532P | 1.50 |
| NE5533P | 1.60 |
| NE5534P | 1.20 |
| NE5534AP | 1.50 |
| OP-07EP | 3.50 |
| PLL02A | 5.00 |
| RC4136 | 0.55 |
| RC4151 | 2.00 |
| RC4195 | 1.50 |
| RC4558 | 0.55 |
| S566B | 2.20 |
| S50240 | 9.00 |
| SAA1900 | 16.00 |
| SFF96364 | 8.00 |
| SL490 | 3.00 |
| SN76013N | 3.00 |
| SN76023N | 3.00 |
| SN76033N | 3.00 |
| SN76115N | 2.15 |
| SN76489 | 4.00 |
| SN76495 | 4.00 |
| SN76660 | 1.20 |
| SPO256AL2 | 7.00 |
| SP8515 | 7.50 |
| TA7120 | 1.20 |
| TA7130 | 1.40 |
| TA7204 | 1.50 |
| TA7205 | 0.90 |
| TA7222 | 1.50 |
| TA7310 | 1.50 |
| TBA641BX1 | 4.00 |
| TBA231 | 1.20 |
| TBA800 | 0.80 |
| TBA810 | 0.90 |
| TBA20 | 0.80 |
| TBA820M | 0.75 |
| TBA920 | 2.00 |
| TBA950 | 2.25 |
| TC9109 | 5.00 |
| TCA210 | 3.50 |
| TCA220 | 3.50 |
| TCA270 | 3.50 |
| TCA940 | 1.75 |
| TDA1004A | 5.00 |
| TDA1010 | 2.25 |
| TDA1022 | 4.50 |
| TDA1024 | 1.10 |
| TDA1170S | 3.00 |
| TDA2002 | 3.25 |
| TDA2003 | 1.90 |
| TDA2004 | 2.40 |
| TDA2006 | 3.20 |
| TDA2020 | 3.20 |
| TDA2030 | 2.50 |
| TDA2593 | 5.00 |
| TDA2653 | 7.00 |
| TDA3560 | 7.50 |
| TDA3810 | 7.50 |
| TDA7000 | 3.50 |
| TEA1002 | 7.00 |
| TL061CP | 0.40 |
| TL062 | 0.60 |
| TL064 | 0.90 |
| TL071 | 0.40 |
| TL072 | 0.70 |
| TL074 | 1.10 |
| TL081 | 0.35 |
| TL082 | 0.55 |
| TL083 | 0.75 |
| TL084 | 1.00 |
| TL094 | 2.00 |
| TL170 | 0.50 |
| TL430C | 1.20 |
| UAA1003-3 | 9.35 |
| UA759 | 3.20 |
| UA2240 | 1.20 |
| UAA170 | 1.70 |
| UCN4801A | 4.00 |
| ULN2001A | 0.75 |
| ULN2002A | 0.75 |
| ULN2003A | 0.75 |
| ULN2004A | 0.75 |
| ULN2068 | 2.90 |
| ULN2802 | 1.90 |
| ULN2803 | 1.80 |
| ULN2804 | 1.90 |
| UPC575 | 2.75 |
| UPC592H | 2.00 |
| UPC1156H | 3.00 |
| UPC1185H | 5.00 |
| XR210 | 4.00 |
| XR2206 | 4.50 |
| XR2207 | 3.75 |
| XR2211 | 5.75 |
| XR2216 | 6.75 |
| XR2240 | 1.20 |
| ZN404 | 1.00 |
| ZN414 | 0.80 |
| ZN419P | 1.75 |
| ZN423E | 1.30 |
| ZN424E | 1.30 |
| ZN425E8 | 3.50 |
| ZN426E8 | 3.00 |
| ZN427E8 | 6.00 |
| ZN428E8 | 4.50 |
| ZN429E8 | 2.25 |
| ZN447E | 9.00 |
| ZN449E | 3.00 |
| ZN450E | 7.50 |
| ZN459CP | 3.00 |
| ZN1034E | 2.00 |
| ZNA1040 | 6.60 |
| ZNA134J | 23.00 |
| ZNA234E | 9.50 |

### VOLTAGE REGULATORS

**1A FIXED VOLTAGE PLASTIC TO220**

| +VE | | −VE | |
|---|---|---|---|
| 5V 7805 | 0.45 | 7905 | 0.50 |
| 6V 7806 | 0.50 | 7906 | 0.50 |
| 6V 7808 | 0.50 | 7908 | 0.50 |
| 12V 7812 | 0.45 | 7912 | 0.50 |
| 15V 7815 | 0.50 | 7915 | 0.15 |
| 18V 7818 | 0.50 | 7918 | 0.50 |
| 24V 7824 | 0.50 | 7924 | 0.50 |

**1A FIXED VOLTAGE PLASTIC TO92**

| | | | |
|---|---|---|---|
| 5V 78L05 | 0.30 | 5V 79L05 | 0.45 |
| 6V 78L06 | 0.30 | 12V 79L12 | 0.50 |
| 8V 78L08 | 0.30 | 15V 79L15 | 0.50 |
| 12V 78L12 | 0.30 | | |
| 15V 78L15 | 0.30 | | |

### OTHER REGULATORS

**FIXED REGULATORS**
LM309K 1A 5V .......... 1.40
LM323K 3A 5V .......... 3.50
78H05KC 5A 5V .......... 5.40
78H12 5A 12V .......... 6.40
78P05 10A 5V .......... 9.00

**VARIABLE REGULATORS**
LM305AH .......... 2.50
LM317T TO-220 .......... 1.50
LM317K TO3 .......... 2.40
LM337T .......... 2.25
LM350T 10A+VAR .......... 4.00
LM396K 10A+VAR .......... 15.00
LM723N .......... 0.50
78HHO5KC 5A 5V .......... 5.75
78HGKC 5A+VAR .......... 6.50
78GUIC 1A+VAR .......... 2.25
79HGKC 5A−VAR .......... 6.75
79GUIC 1A−VAR .......... 2.50

**SWITCHING REGULATIONS**
ICL7660 .......... 2.50
SG3524 .......... 3.00
TL494 .......... 3.00
TL497 .......... 3.00
78S40 .......... 2.50
RC4195 .......... 1.50

## COMPUTER COMPONENTS

**CPU**

| | |
|---|---|
| 1802CE | 6.50 |
| 2650A | 10.50 |
| 6502 | 4.50 |
| 65C02-2MHz | 12.00 |
| 6502A | 6.50 |
| 6502B | 8.00 |
| 6800 | 2.50 |
| 6802 | 3.00 |
| 6803-2 | 12.00 |
| 6809 | 6.50 |
| 6809E | 10.00 |
| 68B09 | 10.00 |
| 68B09E | 12.00 |
| 68000-LB | 36.00 |
| 8035 | 3.50 |
| 80C35 | 6.00 |
| 8039 | 4.20 |
| 80C39 | 7.00 |
| 8080A | 4.20 |
| 8085A | 3.00 |
| 80C85A | 7.50 |
| 8086 | 22.00 |
| 8088 | 17.50 |
| 8741 | 15.00 |
| 8748 | 16.00 |
| TMS1601 | 12.00 |
| TMS9980 | 14.50 |
| TMS9995 | 12.00 |
| Z80 | 2.50 |
| Z80A | 2.90 |
| Z80B | 5.50 |
| Z80H | 7.50 |
| TMS4500 | 14.00 |
| TMS9901 | 5.00 |
| TMS9902 | 5.00 |
| TMS9911 | 18.00 |
| TMS9914 | 14.00 |
| Z80PIO | 2.50 |
| Z80APIO | 2.75 |
| Z80CTC | 2.50 |
| Z80ACTC | 2.75 |
| Z80DART | 6.50 |
| Z80ADART | 7.00 |
| Z80DMA | 7.00 |
| Z80ADMA | 7.50 |
| Z80ASIO/0/2/9 | 7.00 |
| Z80BPIO | 5.00 |
| Z80BCTC | 5.00 |
| Z80BDART | 9.00 |

**SUPPORT DEVICES**

| | |
|---|---|
| 2651 | 12.00 |
| 3242 | 8.00 |
| 3245 | 4.50 |
| 6520 | 3.00 |
| 6522 | 3.50 |
| 6522A | 5.50 |
| 6532 | 4.80 |
| 6551A | 6.00 |
| 6821 | 1.50 |
| 68B21 | 2.50 |
| 6829 | 12.50 |
| 6840 | 3.75 |
| 68B40 | 6.00 |
| 6850 | 1.60 |
| 68B50 | 2.50 |
| 6852 | 2.50 |
| 6854 | 6.50 |
| 68B54 | 8.00 |
| 6875 | 5.00 |
| 8154 | 8.50 |
| 8155 | 3.80 |
| 8156 | 3.80 |
| 8205 | 2.25 |
| 8212 | 2.00 |
| 8216 | 1.60 |
| 8224 | P.O.A |
| 8226 | 4.25 |
| 8228 | 5.50 |
| 8243 | 2.60 |
| 8250 | 9.50 |
| 8251A | 3.25 |
| 8253C-5 | 3.50 |
| 8255AC-5 | 3.20 |
| 8256 | 18.00 |
| 8257C-5 | 54.00 |
| 8259C-5 | 4.00 |
| 8271 | P.O.A |
| 8275 | 29.00 |
| 8279C-5 | 4.80 |
| 8282 | 4.00 |
| 8284 | 4.60 |
| 8287 | 3.80 |
| 8288D | 9.50 |
| 8755A | 16.00 |

**MEMORIES**

| | |
|---|---|
| 216-150 | 4.00 |
| 2101 | 4.00 |
| 2102 | 2.50 |
| 2107B | 5.00 |
| 2111A-35 | 4.00 |
| 2114 | 2.50 |
| 2114-2 | 3.50 |
| 2147 | 4.00 |
| 4116 | 2.00 |
| 4116-20 | 1.50 |
| 41256-207 | 0.50 |
| 41256-157 | 0.50 |
| 4164-15TI | 3.00 |
| 4164 | 2.00 |
| 4164-20 | 2.00 |
| 4416-15 | 3.50 |
| 4532-20 | 2.50 |
| 4816AP/3 | 2.00 |
| 5101/5501 | 4.00 |
| 5514/5114 | 4.00 |
| 5516 | 6.00 |
| 5517AP | 6.00 |
| 6116P-3 | 3.50 |
| 6116LP-3 | 3.50 |
| 6264-12 | 12.00 |
| 6264P-15 | 7.50 |
| 6264LP-15 | 4.00 |
| 6514-45 | 4.00 |
| 6810 | 1.60 |
| 74S189 | 1.80 |
| 74S289 | 2.25 |
| 93415 | 6.00 |
| 93L422 | 7.50 |
| 93425 | 6.00 |

**PROMs**

| | |
|---|---|
| 28L22 | 4.00 |
| 24S10 | 2.50 |
| 18S030 | 2.00 |
| 18SA030 | 2.00 |
| 74S188 | 1.80 |
| 74S287 | 2.25 |
| 74S288 | 1.80 |
| 74S387 | 2.25 |
| 82S23 | 1.50 |
| 82S123 | 1.50 |
| 82S129 | 1.75 |

**EE PROM**

| | |
|---|---|
| 2816-30 | 15.00 |
| 2K+8 | 30.00 |
| 9306 256bits (16×16) | 4.50 |

**EPROMs**

| | |
|---|---|
| 2516+5V | 3.50 |
| 2516-35 | 5.50 |
| 2532 | 4.50 |
| 2532-30 | 5.50 |
| 2564 | 8.00 |
| 2708 | 4.50 |
| 2716+5V | 3.50 |
| 2716-35 | 5.50 |
| 2732 | 4.50 |
| 2732A-2 | 9.50 |
| 2732A-30 | 6.00 |
| 2732A-35 | 5.50 |
| 2764-25 | 2.00 |
| 27C64-25 | 10.00 |
| 27128-25 | 3.00 |
| 27128-25 | 7.50 |
| 27256-25 | 20.00 |
| 27256-30 | 20.00 |
| 17256 | 12.00 |
| 27512 | P.O.A |
| TMS2716 | 5.00 |

**CRT CONTROLLER**

| | |
|---|---|
| CRT5027 | 18.00 |
| CRT5037 | 12.00 |
| CRT6545 | 9.00 |
| EF9364 | 8.00 |
| EF9365 | 25.00 |
| EF9366 | 25.00 |
| EF9367 | 36.00 |
| MC6845 | 6.50 |
| MC6845SP | 6.50 |
| MC6847 | 6.50 |
| SFF96364 | 8.00 |
| TMS9918 | 15.00 |
| TMS9928 | 10.00 |
| TMS9929 | 10.00 |

**INTERFACE ICs**

| | |
|---|---|
| AD7581 | 15.00 |
| ADC0808 | 11.90 |
| AD561J | 20.00 |
| AM25S10 | 3.50 |
| AM25LS2521 | 3.50 |
| AM25LS2538 | 3.50 |
| AM26LS31 | 1.20 |
| AM26LS32 | 1.20 |
| AM7910DC | 25.00 |
| DAC80CB1-V | 28.00 |
| DM8131 | 6.00 |
| DP8304 | 3.50 |
| DS3691 | 3.50 |
| DS8830 | 1.40 |
| DS8831 | 1.50 |
| DS8832 | 1.50 |
| DS8833 | 2.25 |
| DS8836 | 1.50 |
| DS8838 | 2.25 |
| D7002 | 8.00 |
| MC1488 | 0.60 |
| MC1489 | 0.60 |
| MC3446 | 2.50 |
| MC3459 | 4.50 |
| MCS3470 | 4.75 |
| MC3480 | 8.50 |
| MC3486 | 2.25 |
| MC3487 | 2.25 |
| MC4024 | 5.50 |
| MC4044 | 5.50 |
| MC14411 | 9.00 |
| MC14412 | 7.50 |
| 75107 | 0.90 |
| 75108 | 0.90 |
| 75109 | 1.20 |
| 75110 | 0.90 |
| 75112 | 1.60 |
| 75113 | 1.20 |
| 75114 | 1.40 |
| 75115 | 1.40 |
| 75121 | 1.40 |
| 75122 | 1.40 |
| 75150P | 1.20 |
| 75154 | 1.20 |
| 75159 | 2.20 |
| 75160 | 5.00 |
| 75161 | 3.50 |
| 75162 | 4.00 |
| 75172 | 3.00 |
| 75182 | 0.90 |
| 75188 | 0.60 |
| 75189 | 0.60 |
| 75365 | 1.50 |
| 75450 | 0.80 |
| 75451 | 0.50 |
| 75452 | 0.50 |
| 75453 | 0.70 |
| 75454 | 0.70 |
| 75480 | 1.50 |
| 75491 | 0.65 |
| 75492 | 0.65 |
| 8T26 | 1.20 |
| 8T28 | 1.20 |
| 8T95 | 1.20 |
| 8T96 | 1.20 |
| 8T97 | 1.20 |
| 8T98 | 1.20 |
| 81LS95 | 1.40 |
| 81LS96 | 1.40 |
| 81LS97 | 1.40 |
| 81LS98 | 1.40 |
| 88LS120 | 3.00 |
| 9602 | 3.00 |
| 9636A | 1.60 |
| 9637AP | 1.60 |
| 9638 | 1.90 |

**DISC CONTROLLER ICs**

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|---|---|
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| 6843 | 8.00 |
| 8271 | P.O.A |
| FD1771 | 20.00 |
| FD1791 | 20.00 |
| FD1793 | 20.00 |
| FD1797 | 22.00 |
| WD1691 | 15.00 |
| WD2143 | 12.00 |
| WD2793 | 27.00 |
| WD2797 | 27.00 |

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|---|---|
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| 1.00MHz | 2.70 |
| 1.6432MHz | 2.25 |
| 2.00MHz | 2.25 |
| 2.45760MHz(L) | 2.00 |
| 2.45760MHz(S) | 2.50 |
| 2.5MHz | 2.50 |
| 2.662MHz | 1.75 |
| 3.276MHz | 1.50 |
| 3.5795MHz | 1.00 |
| 4.00MHz | 1.50 |
| 4.194MHz | 2.00 |
| 4.43MHz | 1.00 |
| 4.9152MHz | 2.50 |
| 5.00MHz | 1.50 |
| 5.068MHz | 1.75 |
| 6.00MHz | 1.40 |
| 6.144MHz | 1.40 |
| 7.00MHz | 1.50 |
| 7.16MHz | 1.75 |
| 8.00MHz | 1.50 |
| 8.867MHz | 1.75 |
| 10.00MHz | 1.75 |
| 10.50MHz | 2.50 |
| 10.70MHz | 1.50 |
| 11.00MHz | 3.00 |
| 12.00MHz | 1.50 |
| 14.00MHz | 1.75 |
| 14.31MHz | 1.60 |
| 14.756MHz | 2.50 |
| 15.00MHz | 2.00 |
| 16.00MHz | 2.00 |
| 17.734MHz | 1.50 |
| 18.00MHz | 1.50 |
| 18.432MHz | 1.50 |
| 19.969MHz | 1.50 |
| 20.000MHz | 1.50 |
| 24.000MHz | 1.75 |
| 48.000MHz | 1.75 |
| 116MHz | 2.5 |
| PXO1000 | 12.00 |

**OTHERS**

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|---|---|
| 2N5777 | 0.50 |
| BPX25 | 1.80 |
| BPW21 | 2.80 |
| OCP71 | 1.80 |
| ORP12 | 1.20 |
| ORP60 | 1.20 |
| ORP61 | 1.20 |
| SFH205 | 1.00 |
| TIL32 | 0.55 |
| TIL78 | 0.55 |
| TIL31B | 1.20 |
| TIL81 | 1.20 |
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LM3914 3.50
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| | | | | | |
|---|---|---|---|---|---|
| 8pin | 9p | 18pin | 16p | 24pin | 24p |
| 14pin | 10p | 20pin | 18p | 28pin | 26p |
| 16pin | 11p | 22pin | 20p | 40pin | 30p |

**WIRE WRAP SOCKETS BY TI**

| | | | | | |
|---|---|---|---|---|---|
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| 14pin | 35p | 20pin | 60p | 28pin | 80p |
| 16pin | 40p | 22pin | 65p | 40pin | 100p |

**TURNED PIN LOW PROFILE SKTS.**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 8pin | 25p | 16pin | 35p | 20pin | 45p | 28pin | 65p |
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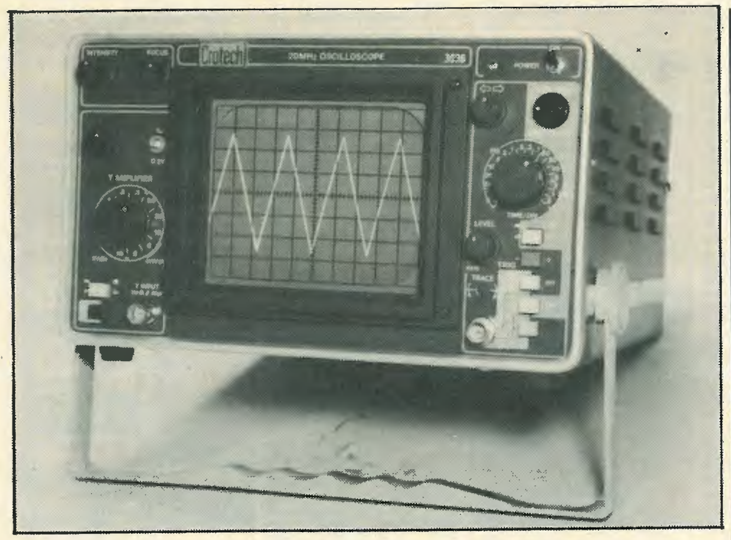


## IEE488 bus controller

Busbox is a simple controller/analyser which can be used in the setting-up and maintaining of IEE488 instrumentation bus systems. The box includes a set of leds which indicate the status of the lines. These are associated with a set of switches which can enable the lines to be forced to a low (or 1) state. The handshake lines are controlled by three-position switches and a pair of pushbuttons which enable Busbox to talk or listen to any device connected to the bus. It operates on 9V supply using an external power supply or internal battery. £99.50 from Peter Levesley Consultancy, 67 Birmingham Road, Aldridge, Walsall, W. Midlands WS9 0AJ. **EWW 207**

## Disc-drive analyser

Combining the functions of a digital storage oscilloscope and a logic analyser, the Nicolet Disc Jockey is an instrument for testing disc drives. A number of built-in test routines may be run to give an accurate assessment of the head alignment, index pulse timing, and rotation speed. A typical inspection test takes about 2min. For design and manufacturing engineers, the instrument offers the option of complete annotation of amplitudes, timing, lobe ratios, and read/write errors and can even offer a prediction as to the long-term reliability of the drive through a 'read window margin' test. A particular feature of the machine is that all the tests are carried out using a graphical display with

preset limits superimposed on the actual performance of the drive under test. The instrument automatically checks whether that performance is within the limits and gives a pass/fail verdict for each test. £7950 from Nicolet Instrument Ltd, Budbrooke Road, Warwick CV34 5XH. **EWW 214**

## Single-trace oscilloscopes

Two new oscilloscopes from Crotech offer the same performance but with different sized screens. 3031 has a 9.5cm c.r.t. and 3036 a 13cm tube. They have a 20MHz vertical bandwidth and 2mV/div. maximum signal deflection coefficient to enable the capture of high-frequency, low-level signals. Timebases are specified from 40ns to 0.2s/div with triggering to over 25MHz in both auto and level modes.

These are combined with the Crotech component tester which allows in or out-circuit testing of active and passive components and extends the use of these oscilloscopes beyond the capabilities of other instruments. Stable operation under adverse mains fluctuation is assured as all supply lines, even e.h.t., are regulated. Crotech Instruments Ltd, 2 Stephenson Road, St. Ives, Huntingdon, cambs PE17 4WJ.

**EWW 215**

## Tandarta workstation

From the modem-maker Tandata emerges an executive workstation, to rival the much-publicised Merlin Tonto and ICL One-Per-Desk. It is British-designed and built and it has some interesting technical features.

To spare the busy executive the tasks of formatting discs, loading them, interpreting the inevitable error-messages and putting them away again, the Tandata P.A. has no magnetic storage at all.

Operating software is all in rom — 128K expandable to 224K — and it passes effortlessly the acid test of user-friendliness by never driving you to look at the manual. Everything is menu-driven: a desk-diary, an address and telephone book, a calculator, a filing system, a text-processor and two-way electronic mail system. Information can be switched instantly from one option into another — for example, a telephone number can be picked out of the address-book and dialled automatically by the built-in loudspeaking telephone.

For data storage, the standard model has 64K of battery-backed cmos ram, expandable to 768K. A compaction feature enables text to be compressed to half its original size. Coloured Prestel graphics pages shrink to about 60%.

The main processor is a 16-bit 80C88, aided by a cmos derivative of the 8-bit 6502 to handle the i/o. The operating system is hidden from the user, but has a multi-tasking Unix-like structure.

The P.A. comes with a colour monitor suitable for 40 or 80-column use; but it has also an l.c.d. screen which enables it to be operated away from base for up to four hours on a built-in rechargeable battery. There is a full range of interfaces, including RS232, i/o expansion bus, printer, cassette, Scart and u.h.f. tv connectors. Prices start at £999. Tandata Marketing Ltd, Albert Road North, Malvern, Worcestershire WR14 2TL. **EWW 217**






## Versatile printer

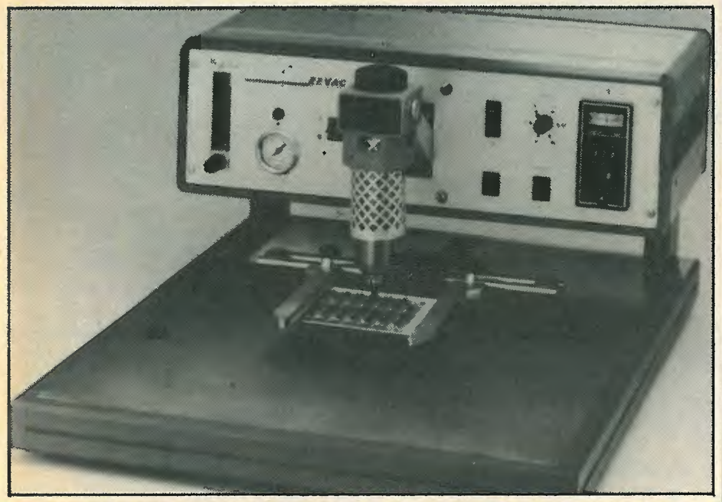
The latest near-letter-quality (n.l.q.) printer from Epson has a special interface cartridge which enables it to be used with Atari, Apple IIc, and IBM computers. Users of these computers had a limited choice of compatible printers. The GX-80 is an alternative to the LX-80 n.l.q. printer. By providing the printer interface cartridge (p.i.c. for £50 extra), the printer may be used with a wide variety of computers with different interface standards.

The printer comes with friction feed (like a typewriter) and can be fitted optionally with a tractor feed and a sheet feeder for multiple copies.

It is provided with a wide selection of print fonts and costs £248. Epson (UK) Ltd, Dorland House, 388 High Road, Wembley, Middlesex HA9 6UH. **EWW 212**

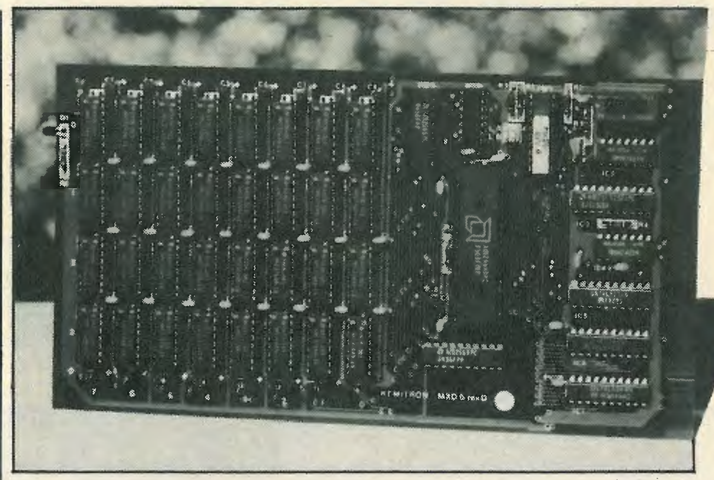
## Desoldering s.m.ds

Zevac DRS-21 is a re-work tool that is designed to desolder and resolder surface-mounted devices on p.c.bs or ceramic substrates. It uses nitrogen gas for heat transfer to give maximum protection to the p.c.b. and components. The gas jets direct heated nitrogen through an interchangeable nozzle to the contact area of the selected s.m.d., positioned using a stereoscopic microscope. The station has a sliding x-y table to position the component and controls for temperature, gas-flow and cycle time. Tony Chapman Electronics Ltd, Electron House, Hemnall Street, Epping, Essex CM16 4LS. **EWW 209**



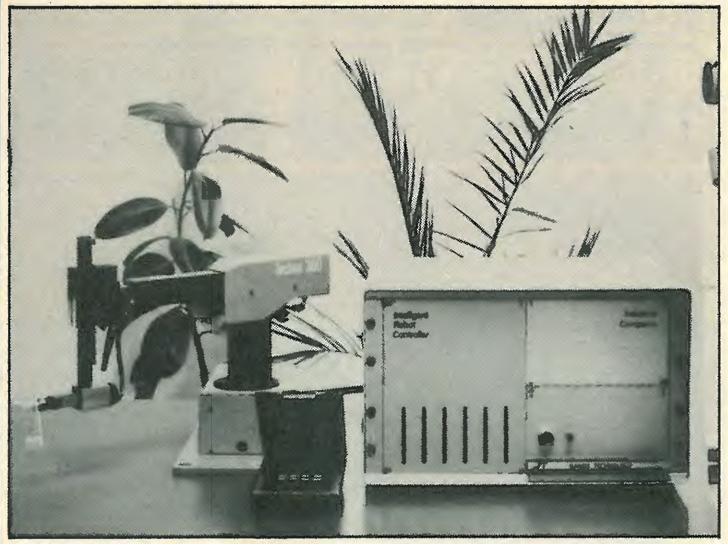

## Automatic pattern maker

Template is a system from Digithurst which can automatically follow the outline of an object with a tv camera and display it on a screen. It is used in conjunction with AutoCad software on the IBM-PC. The user "edits" the image and the software will provide a vectorized sequence so that the pattern can be reproduced automatically by sewing, engraving or cutting machines. One application has been the preparation of plastic signs for hotels and the like where the artwork for the proposed sign is captured and fed into AutoCad. This can produce a cutting sequence in a very short time. Digthurst Ltd, Leaden Hill, Orwell, Royston, Herts SG8 5QH. **EWW 205**



## Ram-disc for CP/M

To speed up data acquisition on a computer, Kemitron have produced a 256K ram card which behaves as if it were a floppy disc. Data can be stored in random access disc files at a rate of up to 18.5Kbytes/s compared with 2Kbyte/s on a floppy drive. Cards may be added to give a capacity of up to 1Mbyte. Data so captured can be transferred to floppy disc for more permanent storage. The ram disc is compatible with the Kemitron range of industrial and scientific computers which use the Z80A processor in a CP/M operating environment. Kemitron Ltd, Hawarden Industrial Park, Manor Lane, Deeside, Clwyd CH5 3PP. **EWW 216**



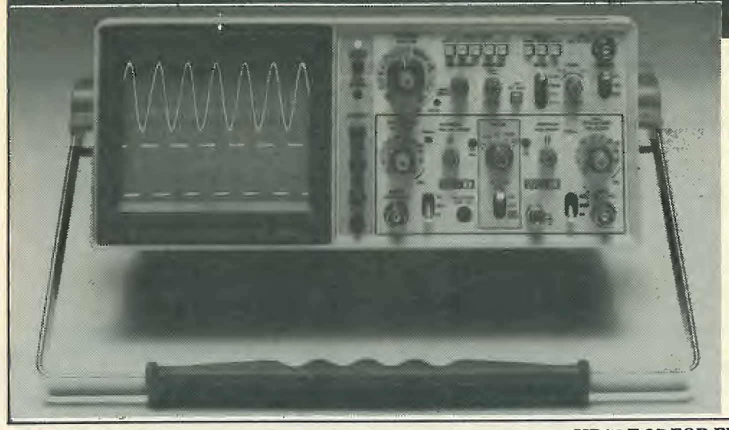
## Robot controller

Up to eight stepper motors can be controlled simultaneously with the robot controller from Sands Technology. Servo systems are being planned. The system controls speed and acceleration of multiple joints with selectable joint interpolation and full cartesian transformations. The program is contained within a 32K battery-backed ram and is based on the resident firmware of Roboforth II control language which provides named places and procedures, motion sub-routines, searching, and many other routines. The language has over 200 commands but, it is claimed, is easy to use and is being increasingly adopted by robot manufacturers. It is available separately as a software package.

With additional plug-in cards, the system will interface with and control other machinery, measurement transducers, etc. and communicate with a mainframe computer. Without the motion control cards, the system may be used as an industrial microsystem and cost less than £1500 including the terminal. As a robot controller, prices vary according to requirements but in a typical application would be about £2,500. Sands Technology, 22 Cheddars Lane, Cambridge CB5 8LD. **EWW 213**

# Hitachi Oscilloscopes

**the highest quality — the most competitive prices — from £299 +VAT**



Hitachi Oscilloscopes provide the quality and performance that you'd expect from such a famous name, with a newly-extended 14 model range that represents the best value for money available anywhere.

| | | | |
|---|---|---|---|
| V-212/222 | 20MHz Dual Trace | V-650 | 60MHz Dual Timebase |
| V-223 | 20MHz Sweep Delay (illustrated) | V-1050 | 100MHz Quad Trace |
| | | V-1070 | 100MHz Four Channel |
| V-209 | 20MHz Mini-Portable | V-1100 | 100MHz DMM/Counter |
| V-422 | 40MHz Dual Trace | V-134 | 10MHz Tube Storage |
| V-423 | 40MHz Sweep Delay | VC-6015 | 10MHz Digital Storage |
| V-509 | 50MHz Mini-Portable | VC-6041 | 40MHz Digital Storage |

Prices start at £299 plus vat (20MHz dual trace) including a 2yr. warranty. **We hold the range in stock for immediate delivery.**

For colour brochure giving specifications and prices ring **(0480) 63570**
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CIRCLE 37 FOR FURTHER DETAILS.

# Add 8 channels to your 'scope

## New Thurlby OM358 multiplexer £179+vat

The Thurlby OM358 gives any oscilloscope an 8 channel display. Observing many waveforms simultaneously can be essential when analysing sophisticated equipment. Application areas include microprocessor based products, data transmission systems, A to D converters, frequency synthesizers etc.
The OM358 is ideal for digital equipment (it can often solve problems that would otherwise need a fast logic analyser) but, unlike dedicated logic test instruments, it is equally suited to analogue waveforms.
The OM358 has a bandwidth of 35MHz and 3% calibration accuracy. Each input has an impedance of 1MΩ - 20pF and accepts signals up to ±6V. An 8 channel, 4 channel, or single channel display can be selected with triggering from any channel. *Colour data sheet with full specifications available.*

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**A complete high performance bench DMM**
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- Full ac and current functions as standard

**A sophisticated computing and logging DMM**
- Linear scaling with offset; null/relative
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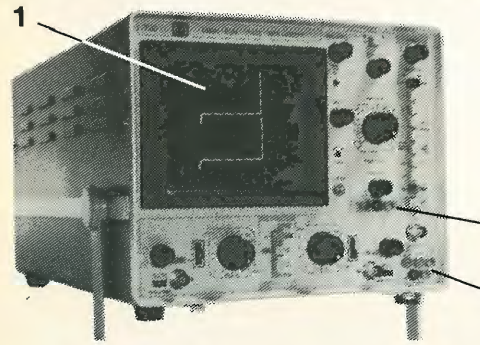


**1 SCOPE:**
DC — 20MHz Bandwidth
2mV/div Sensitivity
40ns — 0.2s/div Sweep
14 Trigger Functions
Including active TV trigger on line & frame.

**2 Active Component Comparator**
(for checking Transistors, diodes and I.C.'s etc)
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**3 Triple Output DC Source**
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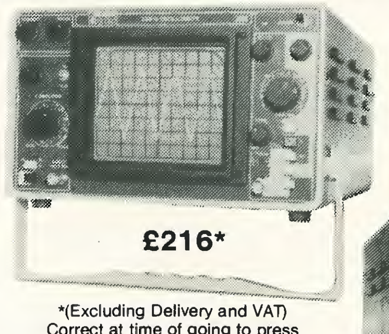
Triggering, Auto and Level
Active Component Tester
Test voltage: 8.6V (28mA)



**£216***

*(Excluding Delivery and VAT) Correct at time of going to press

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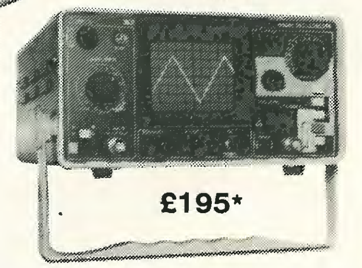
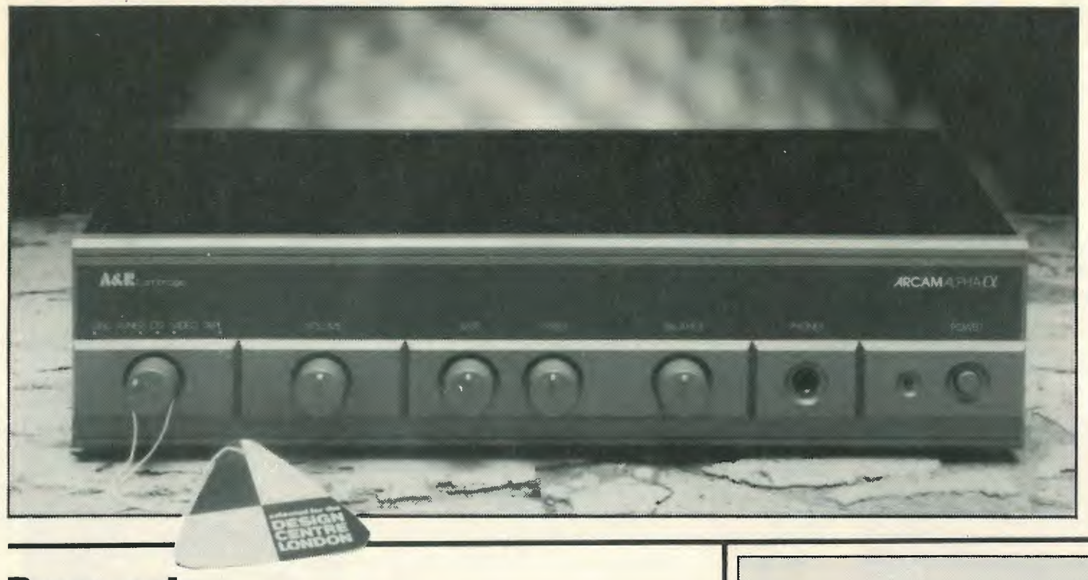
3036 — 130mm CRT
3031 — 95mm CRT



**£195***

**Crotech Instruments Limited**
2 Stephenson Road, St. Ives, Huntingdon, Cambs. PE17 4WJ
Telephone: (0480) 301818
Access
Also available from Audio Electronics & Henry's

CIRCLE 42 FOR FURTHER DETAILS.



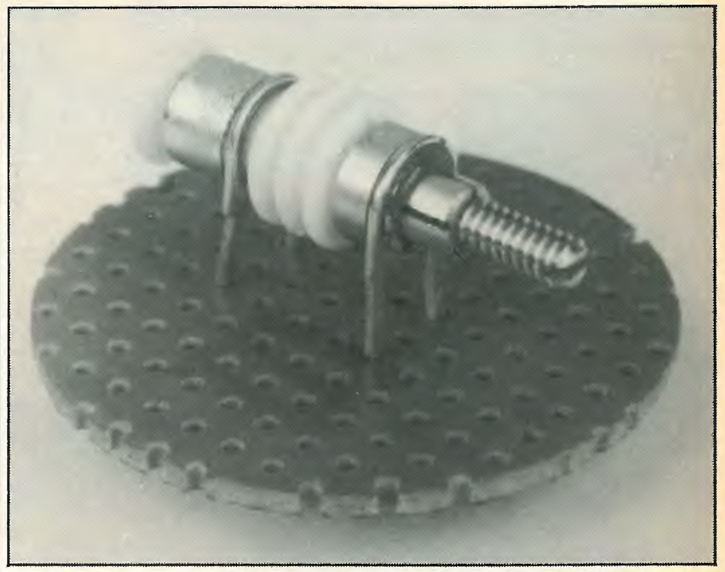

## Design-award amplifier

Arcam Alpha is a low-cost (£130) 30W amplifier which has the distinction of being the first integrated amplifier to be selected for the Design Centre, London. Using many cost-cutting manufacturing techniques, A&R Cambridge claim to have maintained a high quality of performance. It was designed in collaboration with a design consultancy, Cambridge Industrial Design. A stereo tuner at a similar price is to follow. A&R Cambridge Ltd, Denny Industrial Centre, Waterbeach, Cambridge CB5 9PB. **EWW 206**

## Prom-pals

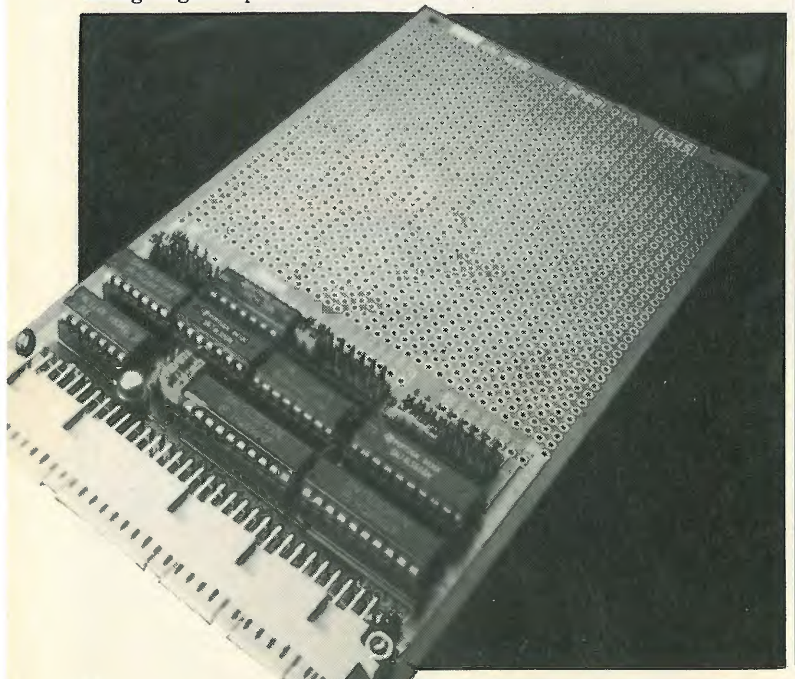
Using fused programmable roms, National have produced a family of programmable array logic chips in a 24-pin package, the series 24A, with up to 20 input lines. The four additional pins over previous similar devices enable more complex functions to be implemented. Examples are 8-bit parallel-in parallel-out counters and shift registers and 16-line to 1-line multiplexers. The devices may be programmed on conventional low-cost prom programmers. Once the pal is programmed and verified, two additional fuses may be blown to defeat further verification. This gives the user a proprietary circuit which is very difficult to copy.

Typically the devices would replace five t.t.l. chips. They make it easier to design boards and save board space and they are easy to program. National Semiconductor (UK) Ltd, 301 Harpur Centre, Horn Lane, Bedford MK40 1TR. **EWW 210**



## Prototyping STE-bus

A bus interface is already fitted to SPC1 Eurocard from Dage but two-thirds of the board is left free for prototyping circuitry. The board is designed for slave i/o applications, and provides selectable address, delay and write timing. Eight chip-select lines and 16 addresses are available which can be used in various ways as required. The standard board has p.t.h. in the prototyping area on a 0.1in pitch. Dage (GB) Ltd, Eurosem Division, Rabans Lane, Aylesbury, Bucks HP19 3RG. **EWW 208**



## High-voltage trimmer capacitor

This trimmer can withstand voltages of 10kV and has a capacitance from 0.5pF with a swing of 3pF. The main components are manufactured from turned p.t.f.e. to give it a diameter of 8mm and a maximum length, at lowest capacitance, of 25mm. Designed to withstand the high r.f. currents used in transceiver equipment, the trimmer is manufactured by Jackson Brothers (London) Ltd, Kingsway, Waddon, Croydon CR9 4DG. **EWW 220** on reply card.

## Driving circuit for laser leds

An 8-pin integrated circuit may be used to control the output of laser diodes. It offers temperature compensation on/off control as well as light intensity, and protects the diodes from poorly regulated power supplies. With a maximum output current of 170mA, the circuit is suitable for use with the Sharp range of semiconductor lasers. The diodes and the IR3C01 driver circuit are available fro Hero Electronics Ltd, Dunstable Street, Ampthill, Beds MK45 2JS. **EWW 205** on reply card.

## Circuit analysis by computer

Jack 17 is software for use with an Apricot computer that has the ability to write and solve the complex equations associated with linear circuits. It is possible to input most of the components directly from a circuit diagram. The program will give a.c. gain and phase response for a specified frequency in a few seconds. Typical applications include filters, amplifiers, matching circuits and attenuators. SpaceHeights Ltd, 6 Prospect Place, Chapelhay, Weymouth, Dorset DT4 8JY. **EWW 211**





## Real time graphs

The Asyst software package enables the IBM PC/XT/AT to monitor, control and analyse data from experiments and production processes, and produce a fast graphical display as it happens. Using the full capabilities of the 8087/80287 co-processor, it is claimed to give the PC the speed and power of a scientific minicomputer, but at a fraction of the cost.

Designed for scientists and engineers, Asyst is said to combine the best features of Fortran, Basic, Pascal, APL, Forth and C, in an integrated package.

The package consists of three modules: (1) system/graphics/ statistics, with editor and help utilities, multiple graphics windows, automatic graph plotting, array editing and a full mathematical function set; (2) analysis, which reduces, manipulates and analyses data: polynomial mathematics and evaluation, vectors and matrices, simultaneous equations; least-squares approximation, data smoothing, integration, peak detection, fast Fourier transforms; (3) data acquisition, giving powerful foreground/background capabilities for analogue and digital i/o, with real-time synchronization, buffered acquisition and triggering, using the Keithley DAS500 data acquisition system.

From Keithley Instruments Ltd, 1 Boulton Road, Reading, Berkshire RG2 0NL. **EWW 224** on reply card.

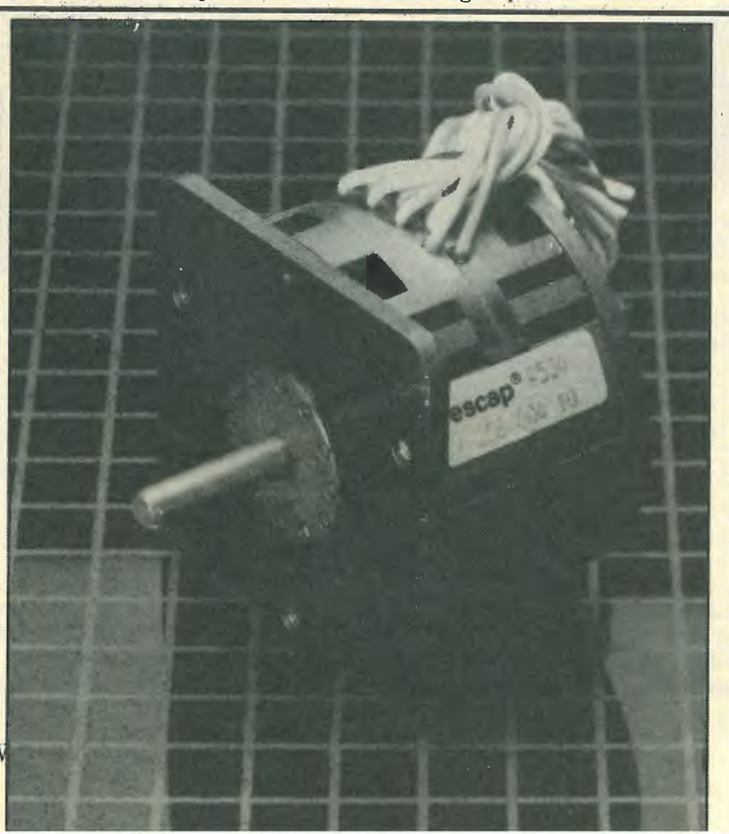

## System tester for micros

A trouble-shooting instrument for microprocessor-based systems is claimed to be easier to use than a logic analyser and, unlike signature analysers, can be used on a completely unserviceable unit. Polar Electronics' B2000A is connected to the unit under test in place of the processor and takes command of the address, data and control lines. It then generates the signals to test rom, ram and i/o ports. Results are reported on the built-in ticket printer. Thirteen pre-programmed tests are available including rom checksum, ram and i/o write and read, dissassemble and search. Of particular value is a test for short circuits which will check any line on the address or data bus with the supply line, ground or any other line. A 'loop' facility enables a test to be repeated continually to allow an oscilloscope to be used to trace a signal path. Tests are stored in non-volatile memory for later use.

B2000A is connected to the system under test through a 'personality' pod which configures the instrument to the specific processor. Pods are available for the Z80, 1802, 6800, 6802, 6809, 8080 and one specifically for the BBC micro. It costs £695 and is available through Antron Electronics Ltd, 39 Kings Road, Haslemere, Surrey GU27 2QA. **EWW 221** on reply card.

## Miniature surface-mounting leds

A series of micro-miniature indicator lamps has been produced measuring 3 by 1.2 by 1mm deep (excluding splayed contacts), designed for direct surface mounting on a p.c.b. The LTL-907 series comes in four versions: red, green, orange and a combined orange/green bi-coloured l.e.d. Each has a luminous intensity of 1.2mcd, measured with a 20mA test current, and a viewing angle of 120°. Information from Selectronic Ltd, The Old Stables, Market Square, Witney, Oxon 0X8 6AL. **EWW 222** on reply card.




## Microstepper motor

A new family of two-phase stepper motors from Portescap is designed to give 800 steps per revolution. This is made possible by increasing the number of poles in the axially magnetized armature disc, and the P530 series offers 100 steps/rev. This is further increased by the phasing of the energizing currents, dividing each step into eight stable microsteps each with an angular displacement of 0.45°.

Three models offer a peak holding torque of 170mNm with only one phase energized and a detent torque of 4mNm, together with a nominal phase current of 0.4 to 3.7A. Portescap UK Ltd, 204 Elgar Road, Reading, Berks RG2 0DD. **EWW 223** on reply card.

CIRCLE 76 FOR FURTHER DETAILS.

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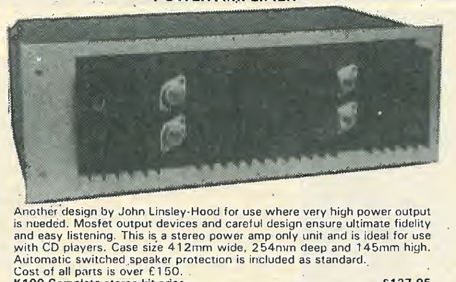

Another design by John Linsley-Hood for use where very high power output is needed. Mosfet output devices and careful design ensure ultimate fidelity and easy listening. This is a stereo power amp only unit and is ideal for use with CD players. Case size 412mm wide, 254mm deep and 145mm high. Automatic switched speaker protection is included as standard.
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**K100 Complete stereo kit price..........................................£127.95**

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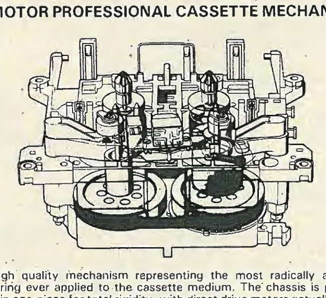

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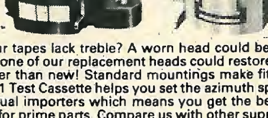

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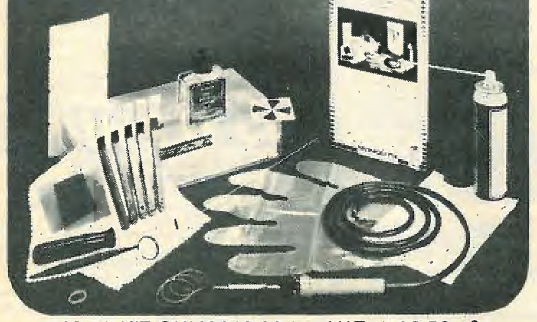

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Little or hardly used manufacturer's surplus enables us to offer this special converted **DECCA RGB** Colour Video TV Monitor at a super low price of only **£99.00**, a price for a colour monitor as yet unheard of!! Our own interface, safety modification and special 16" high definition PIL tube, coupled with well known DECCA 80 series TV chassis give 80 column definition and quality found only on monitors costing **3 TIMES OUR PRICE**. In fact, **WE GUARANTEE** you will be delighted with this product, the quality for the price, has to be seen to be believed!! Supplied complete and ready to plug direct to a **BBC MICRO** computer or any other system with a **TTL RGB** output. Other features are: internal speaker, modular construction, auto degaussing circuit, attractive TEAK CASE, compact dimensions only 52cm W x 34 H x 24 D, 90 day guarantee. Although used, units are supplied in EXCELLENT condition.
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**DECCA 80, 16" COLOUR monitor. Composite video input.** Same as above model but fitted with Composite Video input and audio amp for COMPUTER, VCR or AUDIO VISUAL use. **ONLY £99.00** + Carr.

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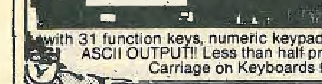

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Brand NEW metal 4 **DISK CASES** with internal **PSU.**

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Supplied **TESTED** in second hand condition complete with **DATA, 50 and 75 baud xtals and large paper roll.**

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(861)

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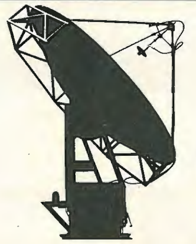

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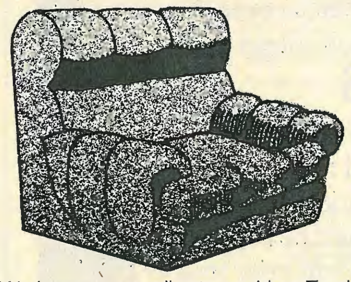

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